A Practical Approach to Commercial Aircraft Data Buses

Revision History

Revision Date	Changes
May, 2010	Inital Release
June, 2010	MIL-STD-1553 Goes Commercial Added
March, 2011	TTP PHY Test Results Added

SUMMARY OF PROPOSED SOLUTIONS

MIL-STD-1553 is a mature field proven technology that provides an ideal solution for emerging commercial aerospace applications. DDC is offering a wide variety of solutions based on this mature technology.

DDC is proposing:

1. MIL-STD-1553
   - Existing 1 Mbps component solutions with 100 million flight hours of in service history available off the shelf today
2. TTP 1553
   - 4 Mbps technology demonstration board exists today
   - Update existing transceiver component to support this higher speed and package with existing TTP controller into a single integrated multi-chip module
3. Turbo 1553
   - Technology demonstrator with MIL-STD-1553 physical and protocol layers running at 3 to 5 Mbps in the lab today
   - Update existing transceiver and protocol components to support this higher speed
4. HyPer-1553
   - Flight worthy technology demonstrator PMC supporting 40 to 200 Mbps exists today
   - Size reduction and conversion of existing double wide PMC into a smaller form factor board product

Commercial Aerospace Data Bus Solutions

MIL-STD-1553

MIL-STD-1553 has been in use in flight and mission critical systems within military aircraft for over 30 years. The continued use of MIL-STD-1553 on new platforms such as F-22 and F-35 is a testament to the reliability of this interface. The current trend in commercial aircraft towards distributed processing architectures in real-time critical systems has created a need for a reliable, deterministic digital data bus. It is only natural that MIL-STD-1553 be considered as a leading candidate for these new commercial aircraft systems.

TTP 1553 – SAE AS6003

Time Triggered Protocol (TTP) is an emerging data bus protocol that is finding its way into commercial aerospace applications. TTP is being released as an SAE Aerospace Standard (AS6003). RS-485 was initially the de facto physical layer for TTP however the performance of RS-485 has been found to be unacceptable for use in avionics applications. The proposed physical layer for AS6003 is MIL-STD-1553, as specified in AS6003 slash 1. DDC has developed a prototype 1553 physical layer interface that operates at 4 Mbps with commercially available TTP controller chips. This prototype physical layer card was used to refine the specifications for AS6003 slash 1.

TURBO-1553

DDC has conducted research aimed at accelerating the speed of MIL-STD-1553 beyond its current 1 Mbps rate. The results of these tests showed that the data rate of MIL-STD-1553 can be reliably increased to 5 Mbps. DDC has developed prototype hardware that demonstrates the performance of a 5 Mbps “Turbo-1553” interface. Turbo-1553 provides an ideal solution for applications that demand the reliable deterministic performance of MIL-STD-1553 but need a slightly higher data rate. Turbo-1553 retains all the architectural benefits of MIL-STD-1553 while operating at a higher data rate.

HYPER-1553

DDC has developed technology called HyPer-1553 that implements high speed digital data communication over legacy MIL-STD-1553 buses utilizing a broadband waveform such that this new high speed communication does not interfere with the legacy 1 Mbps 1553 communication while operating on the same bus. HyPer-1553 supports data rates from 40 to 100 Mbps for concurrent operation depending on bus length and number of nodes. Testing has also shown that data rates of 200 Mbps or higher are feasible on buses where legacy 1 Mbps MIL-STD-1553 communication is not present. HyPer-1553 can be used to implement a high speed multi-drop bus for use in commercial aircraft.

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SECTION 1:

MIL-STD-1553 GOES COMMERCIAL

MIL-STD-1553 Goes Commercial

Introduction

MIL-STD-1553 is a serial data bus that has been used as the primary command and control interconnect in military aircraft for the past three decades. MIL-STD-1553's robust performance, high level of interoperability, large installed based, and well established infrastructure of vendors has made MIL-STD-1553 the network of choice for military avionics systems around the world.

The use of MIL-STD-1553 is not limited to military aircraft. MIL-STD-1553's use is pervasive in military ground vehicles, military ships, UAVs, missiles, and satellite systems. More recently MIL-STD-1553 has been selected for use in the primary flight control system for a commercial aircraft(1). All of these applications share common requirements for a reliable, fault tolerant data bus that will operate in relatively harsh environments. Aircraft applications have unique environmental requirements such as lightning immunity, wide temperature range, high vibration, and high electromagnetic interference (from sources such as radar). MIL-STD-1553 was explicitly designed to operate in these demanding environments.

This paper explores some of the major attributes of MIL-STD-1553 and discusses why MIL-STD-1553 is an ideal choice for use in commercial aircraft systems.

Physical Layer

One of the key architectural features of MIL-STD-1553 is the use of transformers. Transformers are used for two fundamental purposes: galvanic isolation and impedance matching. Galvanic isolation is a major benefit in systems, such as aircraft, that have severe EMI and lightning requirements. Isolation is even more critical in new composite aircraft where the skin of the aircraft no long provides an inherent Faraday shield as was the case with aluminum skinned aircraft.

MIL-STD-1553 defines the topology to be a multi-drop linear bus. Multi-drop buses tend to be lower cost, lower complexity, and lower weight than a switched fabric network. The challenge in implementing a multi-drop bus is to maintain signal integrity to all the receivers on the bus. One of the biggest impediments in a multi-drop bus is reflections. MIL-STD-1553's use of bus couplers is a unique architectural feature that reduces reflections and thus contributes to the performance of this robust physical layer.

Minimizing Reflections

A multi-drop bus starts with a main bus cable that has a characteristic impedance of Z_0 and is terminated into a resistive load equal to Z_0. Transmissions will propagate down the bus and will be dissipated into the termination resistor. Stub cables are then used to connect terminals (communication end points) to the bus. Reflections will occur due to the mismatch in impedance on the main bus caused by the stub connection (refer to Figure 1). Part of the incident wave will be reflected (reflected wave), part will be transmitted up the stub cable (stub wave), and a portion will continue down the transmission line (transmitted wave).

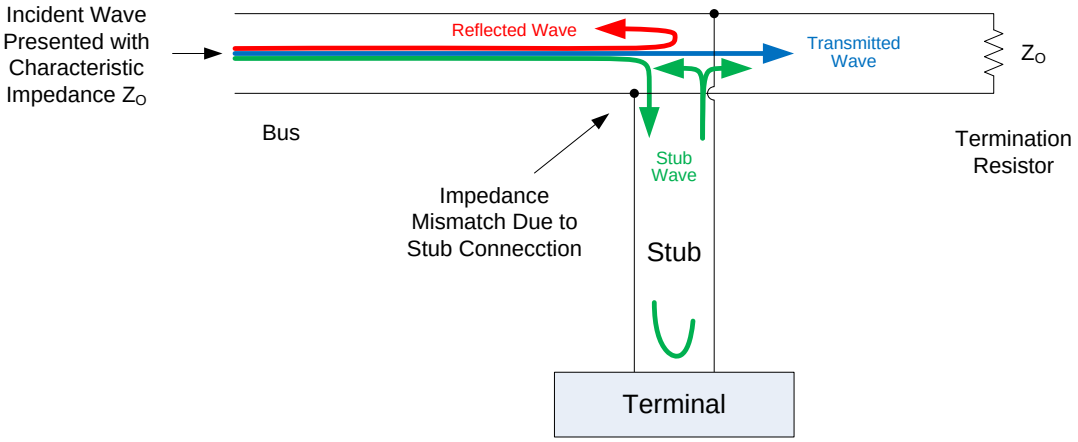

Figure 1. Reflections Caused by Impedance Mismatch

It may be expected that a stub cable be terminated with the characteristic impedance at the terminal interface, however, MIL-STD-1553 defines that the terminal must have a relatively high input impedance. The high input impedance of the terminal relative to the characteristic impedance will produce a large reflection coefficient at the terminal connection to the stub. The result of this high impedance is that most of the stub wave will be reflected back toward the bus and will add back into the incident wave with a phase shift due to the delay down the stub and back. If the terminal were terminated in the characteristic impedance then the signal would be attenuated at every stub connection, and would significantly limit the number of terminals that could be connected to the bus. Instead 1553 minimizes the attenuation due to the stub at the expense of a slight amount of phase distortion.

The amount of reflection on the main bus will be based on the impedance mismatch caused by the stub (refer to Equation 1). The impedance at the stub connection (Z_L) will be a result of the cable's characteristic impedance in parallel with the impedance of the stub. A higher stub impedance will produce a higher Z_L and result in a lower reflection coefficient (C_R).

Equation 1. Reflection Coefficient

$$C_R = \frac{Z_L - Z_0}{Z_L + Z_0}$$

Increasing the impedance of the stub will reduce the amount of reflections on the main bus. The impedance of the stub will be based on the combination of the input impedance of the terminal and the distributed impedance of the cable. Figure 2 illustrates the first –order magnitude calculation of the impedance of the stub as a function of stub length. The figure shows that a 20 foot direct coupled stub with a terminal input impedance of 2000 ohms will result in a stub impedance of less than 300 ohms.

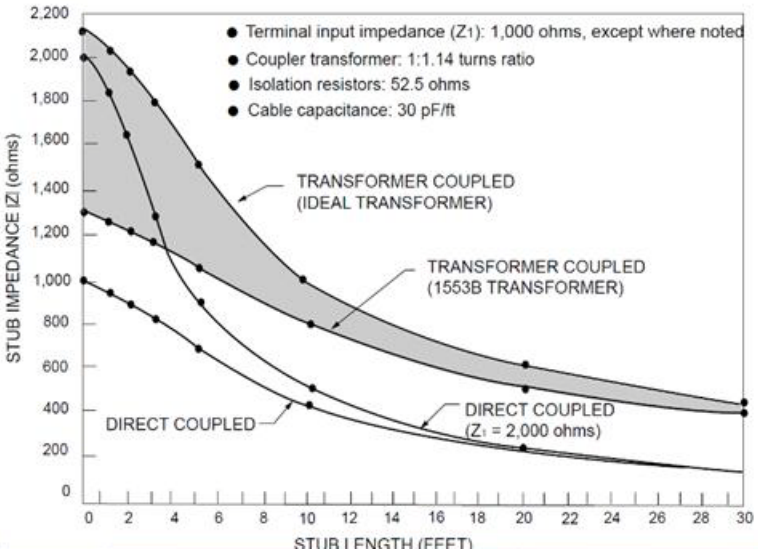

Figure 2. Stub Impedance Versus Stub Length

MIL-STD-1553 defines the option for a transformer coupled connection which utilizes a bus coupler to increase the input impedance of the stub and thus reduce reflections on the main bus. The bus coupler contains a transformer with a turns ratio of 1:1.41 (refer to Figure 3). The transformer will increase the effective impedance of the stub by the turns ratio squared (i.e. by a factor of 2 to 1).

Referring to Figure 2, a transformer coupled terminal will have an input impedance of 1000 ohms. With a stub length of zero the impedance of the terminal will be increased by factor of two (plus the 52.5 ohm series resistors), resulting in an effective stub impedance of 2105 ohms (assuming an ideal transformer). Figure 2 also illustrates the more realistic case using an actual transformer, which will provide an effective stub impedance of approximately 1300 ohms for zero stub length. The real benefit of the transformer coupled connection can be seen with longer stubs lengths. The impedance of a 20 foot stub using transformer coupling will be almost twice the impedance of a direct coupled stub.

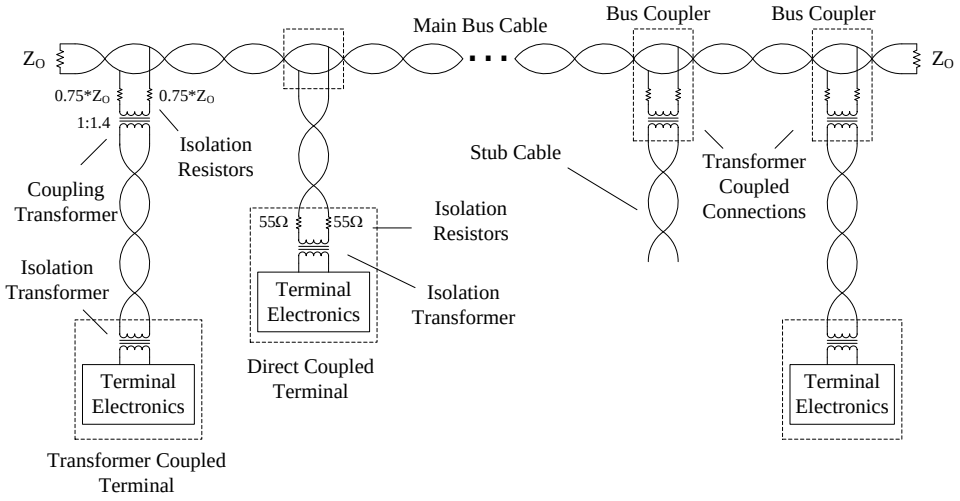

Figure 3. Bus Topology

MIL-STD-1553's transformer coupled connections enable the use of relatively long stubs (up to 20 feet or longer) while still maintaining reasonable transmission line characteristics on the main bus (i.e. minimizing reflections and attenuation).

Fault Isolation

MIL-STD-1553 provides the benefit of fault isolation through the use of series resistors in the path between stubs and the main bus. The fault isolation resistors will allow the network to continue operating even in the presence of a short circuit on one of the stub connections.

Impedance Matching

The values of the isolation resistors and the turns ratio of the coupling transformers are specified such that a matched impedance is presented on the stub input to a bus coupler which helps reduce signal distortion due to secondary reflections on the stub. Refer to Figure 4. A direct coupled terminal will be presented with a bus impedance Z_B which is equal to $Z_0/2$ at the end of the stub. A transformer coupled terminal will be presented with a reflected impedance Z_R through the coupling transformer. The bus impedance for the transformer coupled configuration consists of $Z_0/2$ (termination resistors) in series with two isolation resistors with a value of $0.75 * Z_0$. Therefore the bus impedance Z_B for a transformer coupled terminal will be $Z_0/2 + 2 * 0.75 * Z_0 = 2 * Z_0$. The impedance reflected through the transformer (Z_R) will be increased by the turns ratio squared. $ZR = Z_B/(1.41)^2 = Z_0$. The net effect of the bus coupler is that the impedance from the stub looking into the bus coupler is equal to the characteristic impedance Z_0 which means that the stub is presented with a matched impedance, which will reduce reflections on the stub.

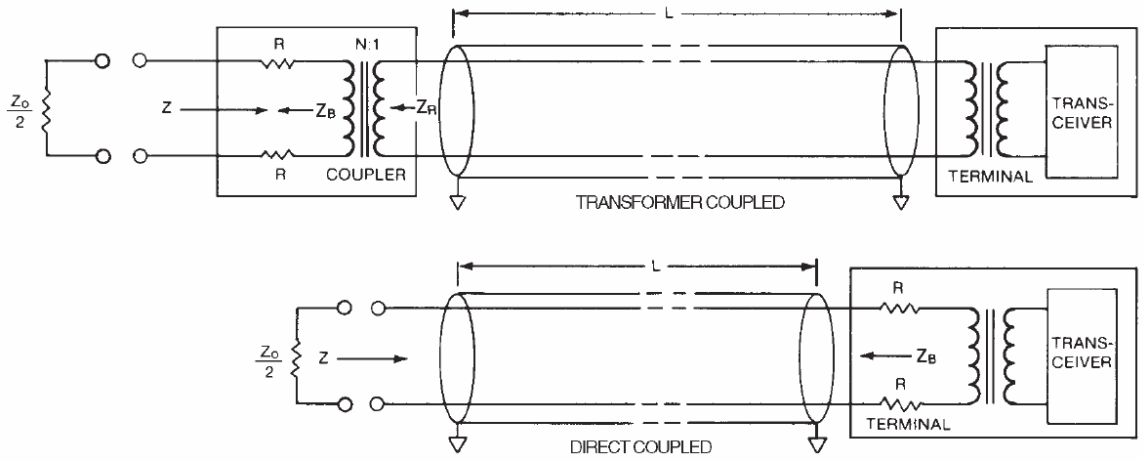

Figure 4. Transformer and Direct Coupled Stubs

MIL-STD-1553 combines stringent transmitter and receiver specifications with a generous link budget to produce a robust data bus that is extremely tolerant to various channel conditions based on bus length, number of nodes, and environmental conditions (such as noise, EMI, and lightning).

Protocol Layer

MIL-STD-1553's use of a command/response protocol enables highly deterministic communication making it ideal for real-time command and control functions, which typically require the transfer of data at a periodic rate (isochronous communication). Every transfer on the bus is initiated by a central bus controller (BC). The centralized bus controller allows the scheduling of data transfers with microsecond accuracy and very low jitter.

Reliable Link Layer

MIL-STD-1553 combines error detection with acknowledgement to implement a reliable link layer protocol. All data transfers on the 1553 bus start with a command word from the BC and include a status response (acknowledgement) from a Remote Terminal (RT). The RT is required to respond to the command within 12 usec. The BC will wait a minimum of 14 usec for the RT response before considering the message to have timed out. Following a timeout the BC has the option of retrying the message either on the same bus or on the redundant bus. 1553's short response timeout value (14 usec) and relatively small payload size (64 bytes max) allow for efficient retransmissions. 1553 also includes support for dual redundancy making it an ideal choice for high availability systems.

Time Synchronization

Many distributed processing systems require time synchronization. MIL-STD-1553 provides the facility for a Remote Terminal to synchronize their local time through the use of the "synchronize" and "synchronize with data" mode codes (protocol specific messages). The synchronize mode code is generally used to reset a local free running counter within the MIL-STD-1553 controller chip while the synchronize with data mode code is used to load the local free running counter within MIL-STD1553 controller with a specific value. Most controller chips, such as DDC's ACE series of components, implement the synchronize mode codes autonomously (without host processor intervention) which enables accurate distribution of time with minimal impact on processor bandwidth. The synchronize mode codes facilitate time partitioning and just in time delivery of data.

Test Plans (Certifiability / In-service History / Maturity

One of the hallmarks of MIL-STD-1553's success over the years has been the high level of interoperability between MIL-STD-1553 interfaces in different boxes. Interoperability is a fundamental requirement for integration of complex systems. Compliance to MIL-STD-1553 is ensured through a suite of validation and production test plans (refer to Table 1). These test plans are published by the Society of Automotive Engineers as Aerospace Standards.

Table 1. Summary of MIL-STD-1553 Compliance Test Plans

AS4111	Validation Test Plan for Aircraft Internal Time Division Command/Response Multiple Data Bus Remote Terminals
AS4112	Production Test Plan for Aircraft Internal Time Division Command/Response Multiple Data Bus Remote Terminals

Table 1. Summary of MIL-STD-1553 Compliance Test Plans	
AS4113	Validation Test Plan for Aircraft Internal Time Division Command/Response Multiple Data Bus Bus Controllers
AS4114	Production Test Plan for Aircraft Internal Time Division Command/Response Multiple Data Bus Bus Controllers
AS4115	Test Plan for the Digital Internal Time Division Command/Response Multiplex Data Bus System

In addition to a rigorous suite of compliance test plans MIL-STD-1553 also has millions of flight hours of in-service history to attest to its reliable operation in an aircraft environment. DDC has estimated that one of their MIL-STD-1553 controller chips has over 65 million flight hours of in-service history. Validation testing and in-service history are important contributors to the design assurance level of systems, especially aircraft systems that will ultimately need to meet the requirements of DO-178 and DO-154.

Conclusion

Why consider a new, unproven technology for use in a flight environment when a mature technology like MIL-STD-1553 is available? The reliability and robustness of MIL-STD-1553 has been proven based on decades of flight history. In addition, MIL-STD-1553 is more cost effective than most people realize. A common misconception is that a 1553 interface is very expensive when in reality the cost of a MIL-STD-1553 node has consistently decreased in price over the last 10 years. MIL-STD-1553 is a natural choice for use in commercial aircraft systems.

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Data Device Corporation is recognized as an international leading supplier of high-reliability data interface products for military and commercial aerospace applications since 1964 and MIL-STD-1553 products for more than 25 years. DDC's design and manufacturing facility is located in Bohemia, N.Y.

References

1. **Data Device Corporation**. 2010 Press Releases. *Data Device Corporation Web Site*. [Online] Data Device Corporation, March 2, 2010. [Cited: March 10, 2010.] http://www.ddc-web.com/News/Press/DDC_Airbus.aspx.

SECTION 2:

MIL-STD-1553 PHYSICAL LAYER FOR TIME-TRIGGERED NETWORKS

09ATC-0129

MIL-STD-1553 Physical Layer for Time-Triggered Networks

Mike Glass
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ABSTRACT

Time Triggered networking technologies such as TTP (Time Triggered Protocol) are beginning to be used in critical aerospace applications such as flight controls. While TTP provides stringent specifications for determinism and fault tolerance, it does not define a physical layer. TTP's "de facto" physical layer, RS-485, includes shortcomings in a number of areas. These include a relatively low minimum transmitter voltage, low receiver threshold, along with a lack of specificity in a number of areas. The latter include bus signal levels, transmitter zero-crossing distortion and receiver zero-crossing tolerance, isolation method, terminal output noise, common mode and noise rejection, and input impedance. MIL-STD-1553, which has been deployed in flight and mission critical military applications for decades, defines a highly proven and robust physical layer. This paper presents MIL-STD-1553's physical layer as a candidate for use with TTP.

INTRODUCTION

Physical layers represent important components for buses and networks used in flight critical applications, with tradeoffs involving topology, data rate, cable length, power, and cost. Time triggered technologies such as TTP (Time Triggered Protocol) and FlexRay use multiple topologies, including multi-drop buses, along with active and passive stars. TTP does not specify a physical layer, resulting in the deployment of multiple implementations rather than use of a common standard.

MIL-STD-1553's multi-drop bus physical layer operates in demanding applications such as flight control, mission computers, and weapons for fighter and attack aircraft. The maturity and technical characteristics of MIL-STD-1553's physical layer make it a strong candidate for use with time triggered networks.

MIL-STD-1553 defines a highly robust and proven physical layer. For use with time triggered technologies, 1553's 1 Mb/s data rate can be scaled to operate at 5 or 10 Mb/s by means of upgraded transceiver and transformer design, and use of 8B/10B encoding.

MIL-STD-1553's physical layer offers many advantages for time triggered networks. These include differential signaling, with a defined "idle" state to help prevent collisions between consecutive transmitters. MIL-STD-1553's use of transformer isolation and optional transformer bus coupling provide DC isolation, common mode rejection, and lightning protection, with series isolation resistors to protect against short circuit faults. The transformer bus coupling option increases stub impedance to enable increased stub lengths.

MIL-STD-1553's relatively high transmit voltages provide strong data rate/cable length performance, while 1553's specifications for rise and fall times limit EMI emissions. Additional 1553 specs include transmitter zero-crossing distortion, overshoot, ringing, droop, output noise, and output symmetry. MIL-STD-1553's output symmetry spec limits the amplitude and duration of "tails" at the end of a node's transmission.

MIL-STD-1553 also defines specs for "must ignore" and "must recognize" receiver voltages, plus requirements for zero-crossing distortion, common mode rejection, noise rejection, and terminal input impedance. MIL-STD-1553B also specifies

voltage ranges delivered by the bus cable to all receiving nodes on the bus. The affect of these latter specs is to impose a maximum loss budget on the bus.

TTP and FLEXRAY -- PHYSICAL LAYERS

Time triggered networks such as TTP (Time Triggered Protocol) and FlexRay deploy multiple topologies. As shown in Figure 1, these include multi-drop bus, active star, passive star, and combinations thereof. Active stars entail penalties in the areas of component volume and weight, cable volume and weight, power, and cost. In these respects, the use of a multi-drop passive bus offers advantages over an active star.

TTP does not define a standard physical layer. This has led to the deployment of multiple physical layers for different implementations, rather than the adoption of a common standard. TTP's "de facto" physical layer, RS-485, includes shortcomings in a number of areas. These include relatively low values for required transmitter voltage and receiver threshold, along with a lack of specificity in a number of specs. The latter include transmitter and receiver zero-crossing distortion, isolation method, bus signal levels, terminal output noise, common mode and noise rejection, and input impedance.

For many decades, MIL-STD-1553 has provided proven and reliable operation in demanding applications such as flight control, mission computers, and weapons control for fighter, attack, and transport aircraft. MIL-STD-1553's maturity and technical characteristics make it a strong candidate as a physical layer for time triggered protocols such as TTP and FlexRay.

MIL-STD-1553 is defined for a 1 Mb signaling rate using Manchester encoding, and therefore a 1 Mb/s data rate. For use with time triggered technologies, 1553's physical layer specifications can be scaled for operation at signaling rates of 5 or 10 Mb.

A basic issue with a multi-drop topology involves the tradeoff between data rate and cable length. This involves loss budget, cable attenuation, stub and node impedances, the number of stubs, and stub lengths. To ensure low bit error rates, multi-drop buses must be defined to provide adequate levels of signal integrity to all receiving nodes.

MIL-STD-1553 defines differential signaling, with three voltage states: idle, active high, and active low. For use with time triggered technologies, the inclusion of an idle voltage level enables receivers to more easily determine "dead time", thereby indicating to the next node to transmit that the bus is "safe"; i.e., there won't be a collision with the preceding node's transmission. Further, the use of a differential, rather than single-ended bus provides advantages in the areas of common mode performance EMI, and lightning immunity. To preclude the possibility of a short circuit fault "taking down" an entire bus, MIL-STD-1553 includes a requirement for all nodes to include series isolation resistors.

DIRECT and TRANSFORMER COUPLING

As shown in Figure 2, MIL-STD-1553 provides two different configurations for coupling a node to a 1553 bus, direct coupling and transformer coupling. It is possible to include a mix of the two types of coupling methods on the same data bus.

MIL-STD-1553 requires the use of transformer isolation for both direct-coupled and transformer-coupled terminals. This provides robustness in the areas of DC isolation, survivability for lightning, and common mode rejection.

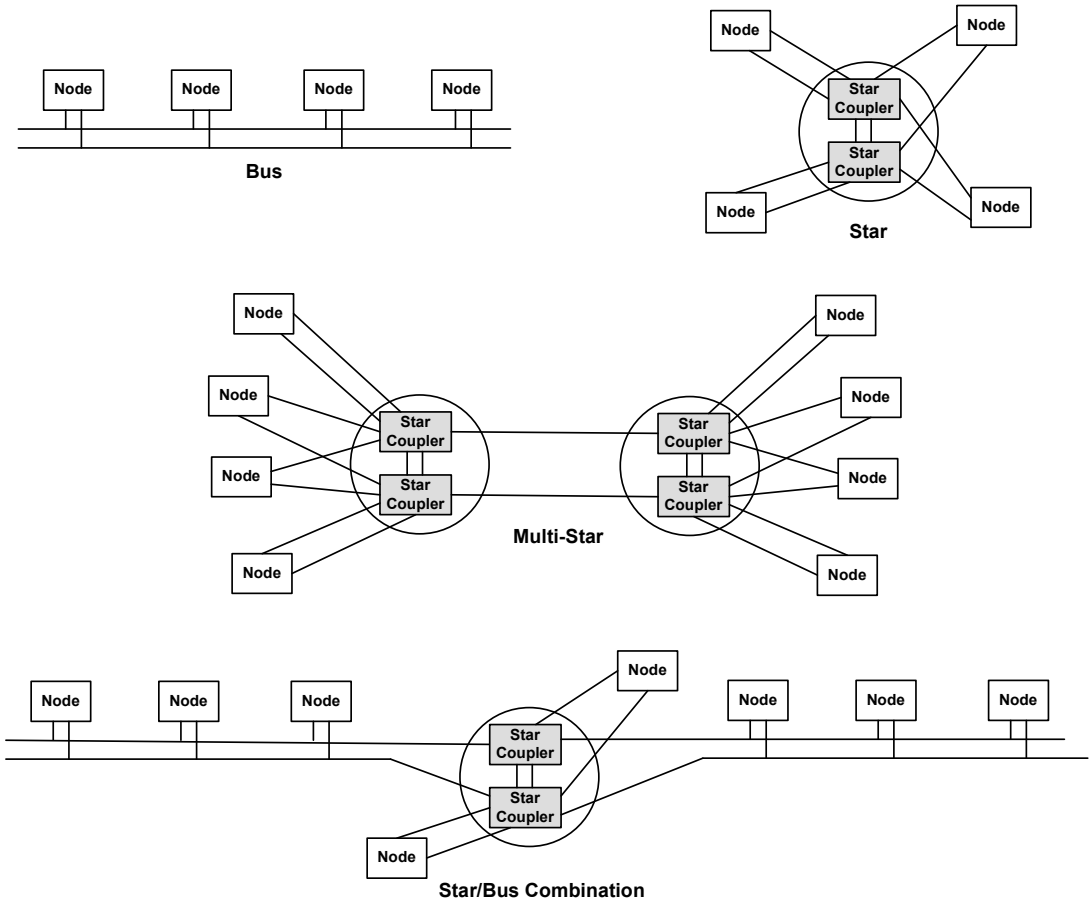


Figure 1. TTP Topologies: Bus, Star, Multi-Star, and Star/Bus Combination[1]

[1] Time-Triggered Protocol TTP/C High-Level Specification Document Protocol Version 1.1, page 21.

Direct coupling includes a requirement for 55 ohm isolation resistors in series with each leg of the isolation transformer. This provides protection in the case of a short circuit in a terminal's transformer or transceiver. If a short circuit occurs, the terminal will load the data bus with 110 ohms, rather than a dead short, allowing the remaining terminals on the bus to continue operation despite the fault. With direct coupling, the recommended maximum distance between the terminal and its connection to the data bus is one foot. The short stub length minimizes the possibility of a short circuit in the sub wiring, which is unprotected by the isolation resistors. In addition, this limitation also minimizes the loading of the data bus from the stub cable's capacitance.

Figure 2 also illustrates MIL-STD-1553 transformer coupling. Transformer coupling entails the use of a bus coupler to interface a terminal's stub to the data bus. As shown, the bus coupler consists of a coupling transformers and a pair of bus isolation resistors. Unlike for direct coupling, there are no isolation resistors in a transformer-coupled terminal. The value of these resistors is $0.75 \bullet Z_0$. These resistors provide protection against short circuit faults in the coupling transformer, stub, and the terminal's isolation transformer and transceiver.

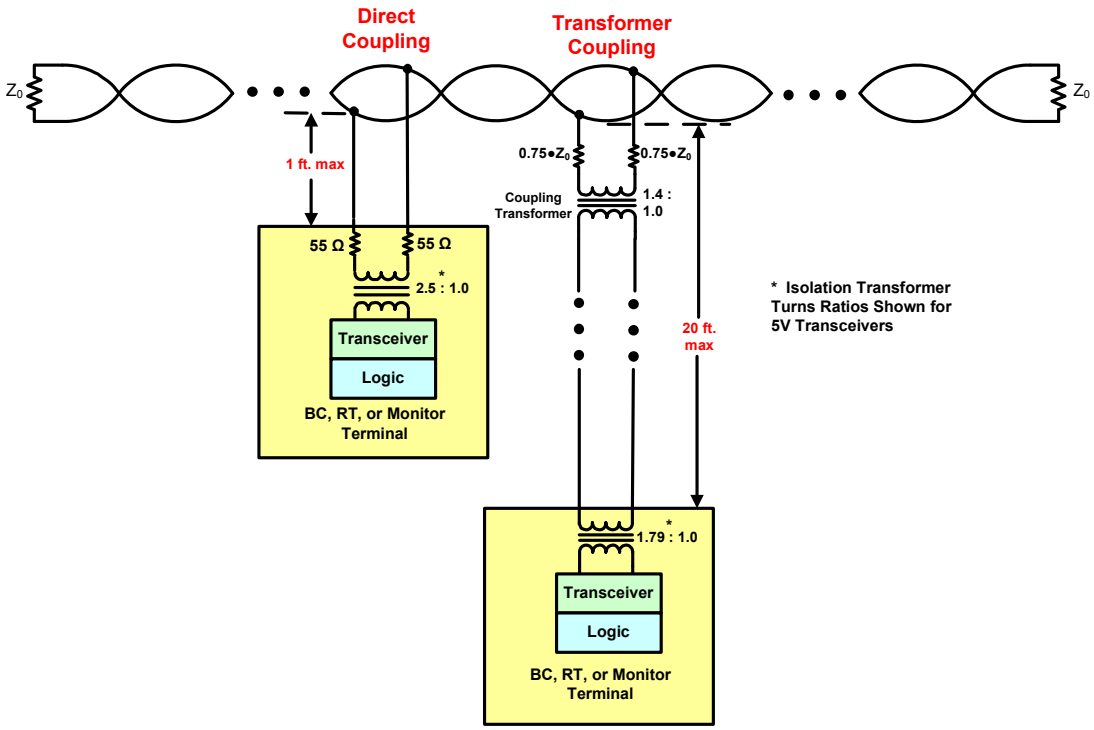


Figure 2. 1553 Direct and Transformer Coupling

MIL-STD-1553 specifies parameters for the coupling transformers, including:

- Turns ratio: 1.4 to 1.0, stepping down, from the bus to the stub.
- Open circuit impedance (on the bus side): ≥ 3,000 ohms, over 75 KHz to 1 MHz.
- Droop: ≤ 20%
- Ringing: ≤ 1 V_{pk}.
- Common mode rejection ratio: ≥ 45 db.

For transformer-coupled terminals, MIL-STD-1553 recommends a maximum distance between the bus and the terminal of 20 feet. Since stub impedance decreases as a function of stub length, the purpose of this recommendation is to limit the bus loading created by individual stubs.

Excessive stub loading increases transmission line reflections, resulting in waveform phase distortion. In addition, increased stub loading tends to reduce the bus voltage.

Transformer coupling enables longer stubs by doubling the stub impedance as "seen" by the main bus cable. In addition, it provides impedance matching for transmitters (the load on the transmitter = Z_0). Further, relative to direct coupling, transformer coupling provides improvements in DC and ground isolation, lightning protection, and common mode rejection.

DATA ENCODING and WAVESHAPING

Figure 3 and Figure 4 illustrate MIL-STD-1553's basic data encoding and waveshaping specifications.

As shown in Figure 3, the encoding method specified by MIL-STD-1553 is Manchester II, or Manchester Biphase-L. For a 1 Mb/s data rate, Manchester encodes a logic '1' as a 500 nS positive voltage, followed by a 500 nS negative voltage; and a logic '0' as a 500 nS negative voltage, followed by a 500 nS positive voltage. In addition to its simplicity, another advantage of Manchester encoding is its transition density. Since Manchester provides a minimum of one signal transition per bit time, this helps to facilitate reliable clock recovery, and the use of oversampling decoding techniques. Further, Manchester encoding provides a balanced waveform with zero DC component, thereby enabling transformer isolation.

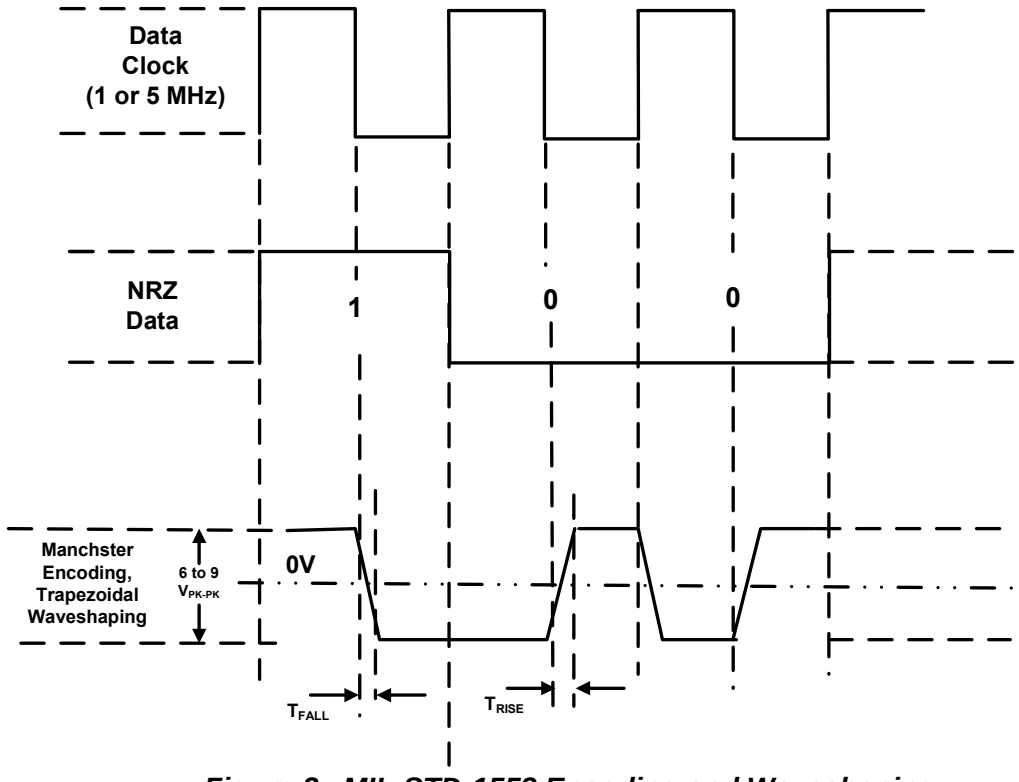


Figure 3. MIL-STD-1553 Encoding and Waveshaping

The 6 to 9 volt peak-to-peak signal amplitude spec shown in Figure 3 refers to the transmitter output for direct coupled terminals. For stub coupled terminals, MIL-STD-1553 specifies 18 to 27 volts across the transmitter stub driving a 70 ohm load. This results in approximately 6.36 to 9.54 volts peak-to-peak driven on to the bus.

As shown in Figure 3 and Figure 4, 1553 specifies trapezoidal waveshaping with a range of rise and fall times of 100 to 300 ns. These times are defined as the transition times between the 10% and 90% points of the peak-to-peak voltage. Trapezoidal, rather than sinusoidal waveshaping, results in simpler transmitter designs, including improved control over the important parameter of zero crossover timing.

The purpose of the lower limit on rise/fall times is to limit the harmonic content of the signal above 1MHz. This serves to minimize EMI and crosstalk, as well as transmission line reflections that can result in false zero crossings and possible decoding errors. Most transmitter designs tend toward the lower limit of the rise/fall time standard as a means of minimizing drive stage power dissipation.

As shown in Figure 4, MIL-STD-1553 limits the overshoot and ringing distortion of the differential transmitted voltage to less than ±300.0 mV peak for direct-coupling, and less than ±900.0 mV peak for transformer coupling. As shown, this spec is applicable for all rise and fall transitions during a transmission, as well following the end the last Manchester half-bit transmitted.

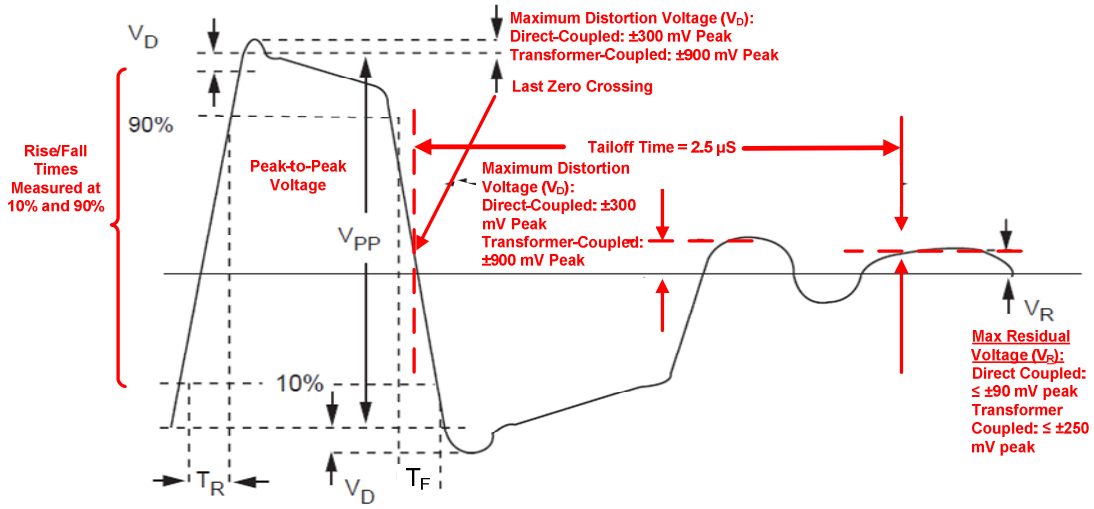


Figure 4. MIL-STD-1553 Transmit Waveform

MIL-STD-1553 includes an additional limit on the distortion at the end of a node's transmission. This spec, commonly referred to as "output symmetry" or "dynamic offset", provides a limit on the residual voltage or "tail". Specifically, this limits the voltage 2.5 µS after the mid-bit zero crossing of the last transmitted bit to less than ±90 mV for a direct-coupled transmitter, or less than ±250 mV for a transformer-coupled transmitter.

For a time-triggered network, this residual voltage spec helps to ensure a "dead bus" following one node's transmission prior to the start of transmission by the subsequent node. A related spec in this respect is that for maximum output noise from a non-transmitting terminal. MIL-STD-1553 limits this to less than 5 mV RMS for a direct-coupled terminal, or less than 14 mV RMS for a transformer-coupled terminal.

ZERO-CROSSING DISTORTION

Figure 5 illustrates another transmitter parameter, zero-crossing distortion. In other networking standards, this is referred to as jitter. Zero-crossing distortion has to do with the time between zero crossings of a Manchester encoded transmitted signal. The times t_{zcp} and t_{zcn} in Figure 5 represent the respective pulse widths of the positive and negative voltage pulses. For MIL-STD-1553 1 Mb/s Manchester encoded signals, the nominal times for t_{zcp} and t_{zcn} are 500 and 1000 nS. Per MIL-STD-1553, the maximum

deviation from these nominal times is ±25 nS; that is, 500 ±25 nS, or 1000 ±25 nS.

In addition to specifying maximum zero-crossing distortion on the transmitting side, 1553 also specifies a minimum tolerance for receivers' zero-crossing distortion tolerance. For t_{zcp} and t_{zcn}, the minimum value of this parameter is ±150 nS. That is, a receiving terminal must accept as valid input signals with zero-crossing distortion of up to ±150 nS. This, together with the ±25 nS tolerance on the transmit side, allows a "zero-crossing distortion budget" of up to ±125 nS that can be introduced as the result of transmission line reflections from stubs, and from the bus cable.

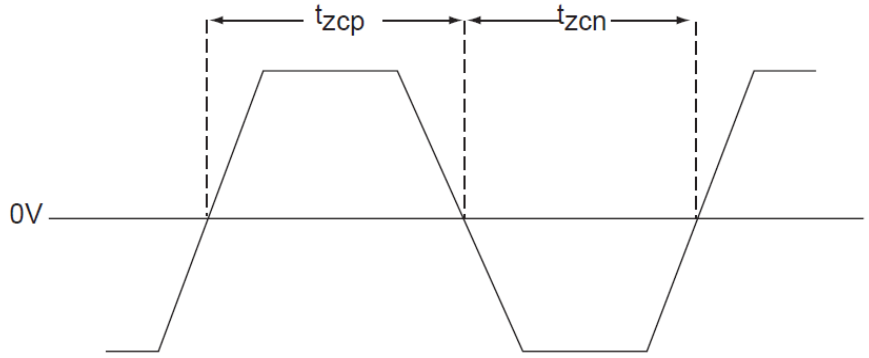


Figure 5. Zero-Crossing Distortion

DATA BUS and RECEIVER VOLTAGES

While MIL-STD-1553A specified a maximum length of 300 feet for the main bus cable, MIL-STD-1553B eliminated this restriction. In its place, as shown in Figure 6, 1553B specifies minimum and maximum voltages that a bus must deliver to all stubs. As shown, a MIL-STD-1553B bus must deliver 1.4 to 20 volts peak-to-peak to all direct-coupled stubs, and 1.0 to 14 volts peak-to-peak to all transformer-coupled stubs. This, in effect, mandates a maximum loss budget for the bus of slightly over 12.6 dB.

MIL-STD-1553B receiver voltage specs are based on the concept of a threshold; that is, the voltage above which a node must consider a received 1553 message to be valid. For direct-coupled terminals, the maximum threshold is 1.2 V peak-to-peak, while for transformer-coupled terminals, the maximum threshold is 860 mV. Relative to the minimum voltage level that must be provided by the bus, this provides a minimum margin of 200 mV peak-to-peak for direct-coupled terminals, and 140 mV for transformer-coupled terminals.

In addition to the maximum threshold voltage, 1553B also specifies minimum "no respond" voltages. That is, received signal levels below this value *must not* be considered to be valid. For direct-coupled terminals, the minimum "no respond" voltage is 280 mV peak-to-peak, while for transformer-coupled terminals, the "no respond" voltage is 200 mV. These "no respond" voltages specify a definitive "dead zone", allowing a node to determine that no other nodes are transmitting. In addition, they provide an inherent degree of noise immunity.

COMMON MODE REJECTION

MIL-STD-1553 specifies a minimum level of common mode rejection for all terminals. Common mode rejection is partially a characteristic of the terminals' isolation transformers, and is a form of noise disturbance commonly encountered in avionics.

As shown in Figure 7(a), for the common mode test for a transformer-coupled terminal, the common mode signal is applied between the center tap of the bus coupling transformer on the "stub" side and ground. As shown in Figure 7(b), for a direct-coupled terminal, the common mode signal is applied between the junction of two "half-

termination" resistors (0.5●Z_0 each) and ground.

For the terminal common mode rejection test, the minimum signal level of 860 mV peak-to-peak transformer-coupled, or 1.2 V direct-coupled is used. The common mode signal applied includes ±10 VDC, and a ±10 V (peak) AC voltages whose frequency is swept from 1 Hz to 2 MHz. To pass, the terminal must accept all messages received.

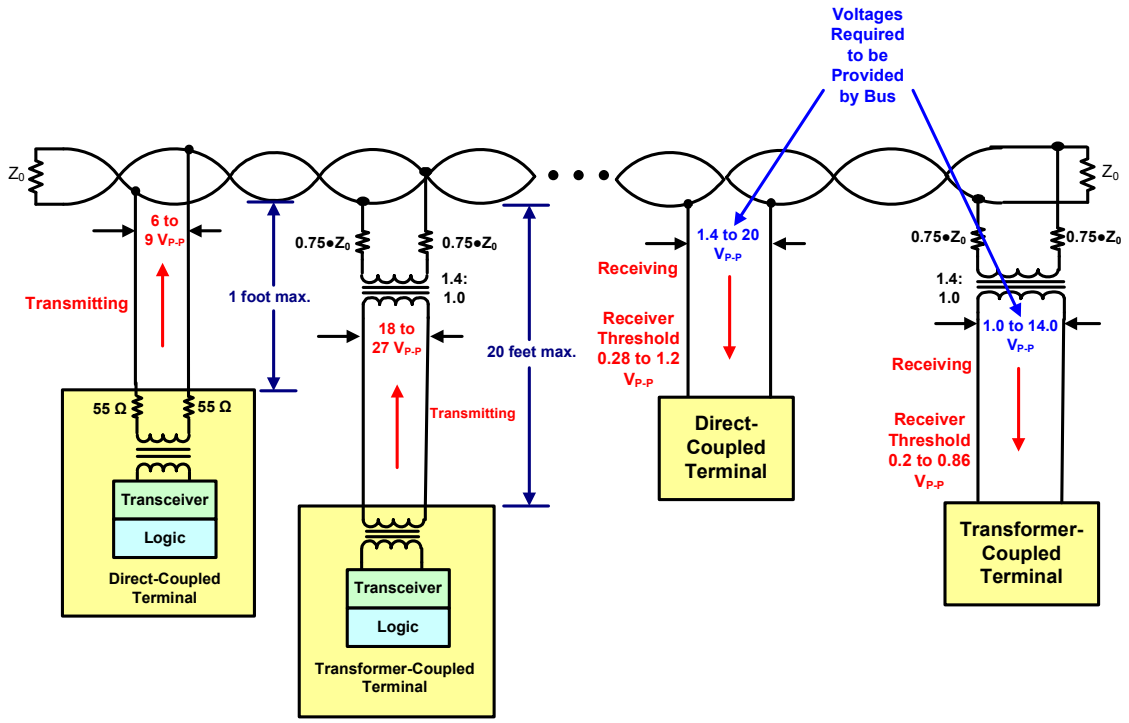


Figure 6. MIL-STD-1553 Bus, Stub, and Receiver Voltages

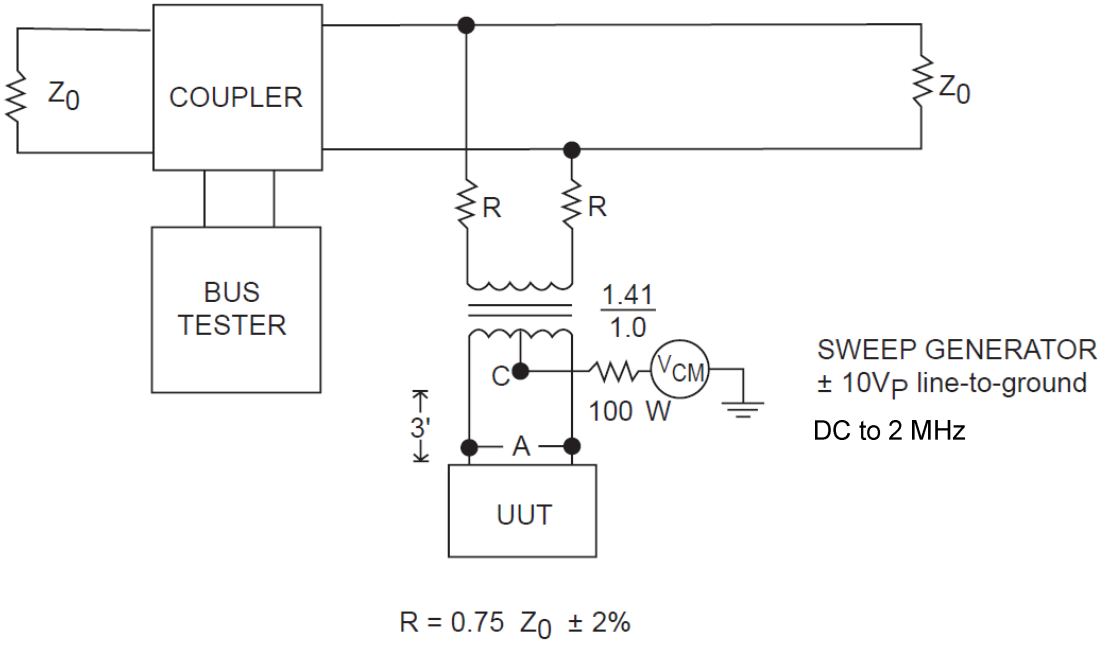
INPUT IMPEDANCE

Another 1553 physical layer spec is terminal input impedance. The importance of input impedance is that it effects the loading on the main bus. Excessive stub loading increases transmission line reflections, resulting in waveform phase distortion, and tends to reduce the bus voltage. MIL-STD-1553 specifies a minimum terminal input impedance over the frequency range of 75 KHz to 1 MHz. This represents the range of fundamental frequencies for 1553 signals.

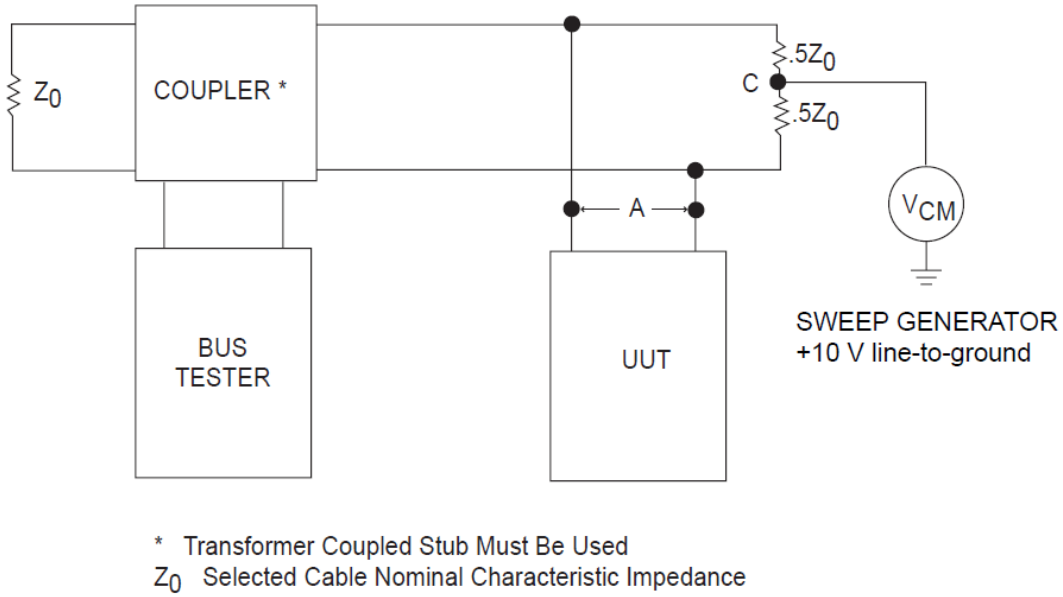
For direct-coupled terminals, the terminal input impedance must be a minimum of 2,000 ohms, while for transformer-coupled terminals, the terminal input impedance must be a minimum of 1,000 ohms. The reflected impedance of transformer-coupled terminals to the main bus is doubled by the 1.4 to 1.0 turns ratio of the bus coupling transformer.

NOISE REJECTION (BIT ERROR RATE)

Another spec for 1553 terminals is noise rejection, or bit error rate testing. MIL-STD-1553B defines a test for terminals to be able to receive messages in the presence of white, Gaussian noise applied differentially across the data bus or stub. This test, which is defined within the 1553 standard, provides a figure-of-merit test criteria for operating in an environment including switching power supplies, radios, radar, electromechanical switching, and other sources of EMI.



(a)



(b)

Figure 7. MIL-STD-1553B Common Mode Rejection Test: (a) Transformer- coupled; (b) Direct-coupled[2]

[2] SAE AS4111; Validation Test Plan for the Digital Time Division Command/Response Multiplex Data Bus Remote Terminals; Figure 6A, page 60; and Figure 6B, page 61.

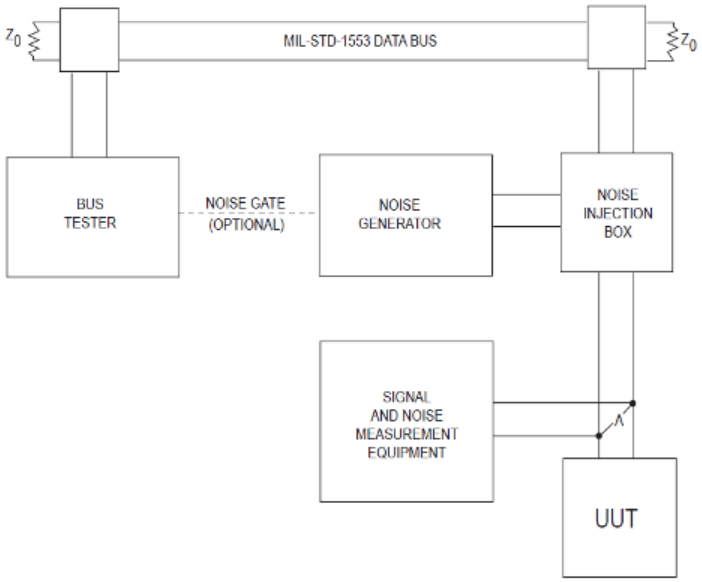


Figure 8. Noise Rejection (Bit Error Rate) Test

The 1553 noise test specifies signal and noise levels, with a signal-to-noise ratio of approximately 16.6 dB. For direct-coupled terminals, the test entails the use of a signal level of 3.0 volts peak-to-peak and a white Gaussian noise source of 200 mV RMS distributed over 1.0 to 4.0 MHz. For transformer-coupled terminals, the test specifies a signal level of 2.1 volts peak-to-peak and a white Gaussian noise source of 140 mV RMS.

In both cases, the terminal must demonstrate a word error rate of less than 10^{-7}., equivalent to a bit error rate of $2 \bullet 10^{-9}$.

BUS ISOLTION

To ensure independence for redundant buses, MIL-STD-1553 specifies a minimum isolation of 45 dB between buses.

VALIDATION TESTING

One of the keys to MIL-STD-1553's long-term success in military use is its defined and publically available criteria for validation testing. This delineates a rigorous suite of tests, to which a terminal must demonstrate compliance to. This test includes all of the physical layer parameters discussed in this paper, along with comprehensive protocol testing. As a result, while MIL-STD-1553 has been implemented by many dozens of different designers over the years, it has historically *not* encountered issues with interoperability.

CABLE

MIL-STD-1553's cable specifications include the use of twisted/shielded cable, with a defined characteristic impedance, maximum attenuation, shielding coverage, capacitance, twists per foot, and EMC. Table 1 lists MIL-STD-1553's cable characteristics.

Table 1. MIL-STD-1553 Cable Characteristics

Property	Value

Type	Twisted-shielded pair
Characteristic impedance (Z_0)	70 to 85 ohms at 1.0 MHz
Attenuation	1.5 dB/100 ft at 1.0 MHz, maximum
Shielding Coverage	75% minimum
Length of main bus	Not specified
Capacitance (wire to wire)	30 pF/ft, maximum
Twist Four per foot	0.33/in, minimum
EMC	Per MIL-E-6151

COMPARISON: MIL-STD-1553 vs. RS-485

Like MIL-STD-1553, RS-485 is based on the use of differential signaling. However, in many respects, RS-485 is a less robust standard than 1553. For example, RS-485's minimum bus voltage is 1.5 volts peak (3.0 volts peak-to-peak), which is half of the MIL-STD-1553 minimum bus voltage of 6.0 volts peak-to-peak. Similarly, in order to provide a degree of noise immunity, 1553 specifies higher voltages for receiver threshold than RS-485, including (in effect), "must reject" voltages.

For rise and fall times, in order to control EMI emissions, MIL-STD-1553 specifies both a minimum and maximum, while 485 specifies only a maximum. In addition, while MIL-STD-1553 provides a clear delineation of bus "dead time", RS-485 does not.

Further, 1553 defines specs in a number of areas for which RS-485 is "silent" about. These include isolation method and options for either direct or transformer coupling; ranges for bus voltages delivered to receivers (loss budget); transmitter limitations and receiver tolerances for zero-crossing distortion (jitter); noise rejection (bit error rate); and terminal input impedance.

Table 2 provides a comprehensive comparison of MIL-STD-1553's physical layer relative to RS-485.

Table 2. Physical Layer Comparison: MIL-STD-1553 vs RS-485

Characteristic	MIL-STD-1553	RS-485	Advantage/Benefit
Type of Signaling	Differential	Differential	**Even.** Both MIL-STD-1553 and RS-485 use differential signaling.
Signal Encoding Method	Manchester Bi-Phase	Not specified.	**N/A**
Transmit Voltage	Direct Coupled: 6.0 to 9.0 V_{PK-PK} Transformer Coupled: 18.0 to 27.0 V_{PK-PK}	Differential voltage = 1.5 to 5.0 volts = 3.0 to 10.0 V_{PK-PK}	**MIL-STD-1553.** For both direct and transformer-coupled configurations, MIL-STD-1553 provides a higher minimum bus voltage: 6.0 V_{PK-PK} direct-coupled, or 6.36 V_{PK-PK} transformer-coupled.
Rise/Fall Times (10% to 90%)	100 to 300 nS	≤0.3●UI	**MIL-STD-1553.** For MIL-STD-1553, a stream of all Manchester "1"s or "0"s results in rise/fall times in the range of 0.2●UI to 0.6●UI. For alternating "1"s and "0"s, the corresponding rise/fall times are 0.1●UI to 0.3●UI. MIL-STD-1553's upper limit is equivalent to that for RS-485. MIL-STD-1553's lower limit of 100 nS serves to minimize EMI and over/undershoots.
Transmitter Zero-Crossing Deviation	≤ ±25 nS	Not specified	**MIL-STD-1553.** MIL-STD-1553 specifies an upper bound on transmit jitter, thereby providing increased margin for distortion introduced by bus cabling and stubs.
Non-Transmitting Output Noise	Direct Coupled: ≤ 5 mV RMS line-to-line Transformer Coupled: ≤ 14 mV RMS line-to-line	Defines a maximum offset voltage in the range of -1.0 to +3.0 volts.	**MIL-STD-1553.** MIL-STD-1553's more stringent requirement for non-transmitting output voltage guarantees a lower maximum level of interference from inactive (non-transmitting) nodes.
Output Symmetry – Residual Voltage	Direct Coupled: ≤ 90 mV peak, line-to-line Voltage 2.5 µS after last mid-bit crossing Transformer Coupled: ≤ 250 mV peak, line-to-line Voltage 2.5 µS after last mid-bit crossing	Maximum common mode voltage is -3.0 to +1.0 volts. Maximum difference between positive and negative peak voltages must be ≤ 0.2 volts.	**MIL-STD-1553.** MIL-STD-1553's requirement for a maximum residual (or "tailoff") voltage 2.5 µS following the end of a transmission ensures non-interference with the subsequent transmission on the bus. In addition, RS-485's allowance for a DC offset voltage complicates the use of transformer isolation.
Node isolation.	Isolation transformers are required for all MIL-STD-1553 terminals.	Isolation is not required.	**MIL-STD-1553.** MIL-STD-1553's requirement for transformer isolation ensures a high degree of ground isolation, and lightning and common mode rejection.
Bus-to-Bus Isolation	≥ 45 dB	None	**MIL-STD-1553.** MIL-STD-1553 limits crosstalk between redundant buses.
Fault Isolation	Direct Coupled: 55 ohm Series Resistors in Each Terminal Leg	None	**MIL-STD-1553.** The requirement for isolation resistors prevents a short-circuited terminal or stub from taking the entire bus out of operation.

Characteristic	MIL-STD-1553	RS-485	Advantage/Benefit
	Transformer Coupled: 0.75●Z_0 Series Resistors in Each Stub Leg		
Bus Coupling Transformer	Turns Ratio: 1.4 to 1.0 (step-down, bus to stub)	N/A	**MIL-STD-1553.** The option for transformer coupling provides increased stub impedance, matched transmitter impedance, improved ground isolation, and provides a higher degree of lightning immunity.
	Open Circuit Impedance: ≥ 3,000 ohms, over 75 KHz to 1 MHz		
	Droop: ≤ 20%		
	Ringing: ≤ 1V peak		
	Common Mode Rejection: ≥ 45 dB		
Signal Level Delivered By Bus to Stub	Direct Coupled: 1.4 to 20 V_{PK-PK}, line-to-line	Not specified	**MIL-STD-1553.** MIL-STD-1553A specified a maximum cable distance of 300 feet. While MIL-STD-1553B dropped this requirement, it requires a minimum (and maximum) voltage to be presented to each terminal and/or stub on the bus. This forces implementers to design terminals, buses and stubs in such a way to ensure reliable network operation.
	Transformer Coupled: 1.0 to 14 V_{PK-PK}, line-to-line		
Receiver Signal Range	Direct Coupled: 1.2 to 20 V_{PK-PK}, line-to-line	-0.2V (peak) ≤ threshold voltage ≤ +0.2V (peak). This implies a receiver "threshold" of 0.0 to 0.4 volts peak-to-peak.	**MIL-STD-1553.** MIL-STD-1553 allows higher receiver thresholds than RS-485, thereby providing a lower bit error rate. Further, MIL-STD-1553 receivers must provide a "dead zone" of 0.28 V V_{PK-PK} = ±0.14 V_{PK} (direct coupled), or 0.2 V V_{PK-PK} = ±0.1 V_{PK} (transformer coupled), thereby providing improved noise immunity. In addition, this improves the capability for a 1553 receiver to be able to determine the end of a received signal transmission. For TTP, this enables shorter gap times between transmissions by individual nodes. RS-485's minimum receiver threshold of 0V can result in receiver output jitter when there is no received signal.
	Transformer Coupled: 0.86 to 14 V_{PK-PK}, line-to-line		
Receiver "No Response" Range	Direct Coupled: 0 to 0.28 V_{PK-PK}, line-to-line		
	Transformer Coupled: 0 to 0.2 V_{PK-PK}, line-to-line		
Receiver Zero-Crossing Distortion Tolerance	≥ ±150 nS	Not specified.	**MIL-STD-1553.** This 1553 requirement provides tolerance for phase shifts introduced by transmitters, bus cabling and stubs.
Receiver Common Mode Rejection	± 10 V_{PEAK}, line-to-ground, DC to 2 MHz	Receivers must operate over a common mode voltage range of -7V to +12V	**MIL-STD-1553.** MIL-STD-1553's common mode range is slightly higher, ±10V_{PK} = 20 V_{PK-PK} vs. RS-485's of +12/-7 V_{PK} = 19 V_{PK-PK}. In practice, MIL-STD-1553's requirement for transformer isolation

Characteristic	MIL-STD-1553	RS-485	Advantage/Benefit
	For transformer-coupled stubs, coupling transformers must have a common mode rejection ratio greater than 45.0 dB at 1.0 MHz.		provides a greater common mode rage than ±10V_{PK}. In addition, MIL-STD-1553's option for transformer coupling with a common mode rejection ratio of 45 dB for coupling transformers provides a further improvement in overall common mode rejection.
Noise Rejection (Word Error Rate)	Direct Coupled: ▪ 3.0 V_{PK-PK} Signal Level ▪ 200 mV RMS White Gaussian Noise, 1.0 to 4.0 MHz ▪ Word Error Rate < 10^{-7} Transformer Coupled: ▪ 2.1 V_{PK-PK} Signal Level ▪ 140 mV RMS White Gaussian Noise, 1.0 to 4.0 MHz ▪ Word Error Rate < 10^{-7}	No specified	**MIL-STD-1553.** MIL-STD-1553's noise rejection (bit error rate) test ensures the implementation of receiver filtering, thereby providing reliable operation in the presence of differential noise.
Terminal Input Impedance	Direct Coupled: ≥ 2,000 ohms, over 75 KHz to 1 MHz Transformer Coupled: ≥ 1,000 ohms, over 75 KHz to 1 MHz	Defines the concept of "unit load", in which a receiver's, transmitter's, or transceiver's DC resistance is approximately 8.7 KΩ to 12 KΩ. A receiver's, transmitter's, or transceiver's overall input impedance, including reactive (i.e., capacitive) components, is not specified. In addition, the input resistance can be either less than, equal to, or greater than one "unit load".	**MIL-STD-1553.** MIL-STD-1553's minimum values for terminal impedance provide a limitation of the bus voltage loading by individual terminals, and minimize distortion resulting from transmission line reflections.

CONCLUSION

Currently, TTP (Time Triggered Protocol) does not specify a physical layer standard. The physical layer defined by MIL-STD-1553 is a strong candidate for use with time triggered networking technologies such as TTP and FlexRay. In particular, MIL-STD-1553 provides higher transmit voltages and receiver thresholds relative to RS-485. In addition, 1553 provides detailed specifications in a number of areas which are not defined by RS-485, including transmitter zero-crossing distortion and receiver zero-crossing tolerance, isolation method, terminal output noise, common mode and noise rejection, and input impedance.

MIL-STD-1553's higher bus voltages and other specs make it highly suitable for use in a passive, multi-drop topology. Use of a passive, multi-drop topology reduces or eliminates the need for active star couplers, thereby leading to reductions in the associated total cable length, cost, power, weight, and volume.

MIL-STD-1553 Physical Layer (PHY) for TTP – Test Results

Introduction

Time Triggered Protocol (TTP) is emerging as a strong candidate for use in real-time distributed processing control systems in commercial aircraft. Early implementations of TTP in commercial aircraft have faced challenges meeting the environmental requirements of an aircraft, especially lightning and HIRF. RS-485 has been the de facto physical layer for TTP yet a detailed analysis found RS-485 to be lacking is several key areas. RS-485 suffers from a low transmit signal, low receiver threshold, inadequate isolation method, short stub length and is non-specific in many areas (interoperability issues).(1)

MIL-STD-1553 is a 1 Mbps deterministic serial data bus that has been in use in real-time critical systems in military aircraft for over 30 years. MIL-STD-1553 was designed specifically for use in an aircraft environment and as such provides robust performance in terms of isolation and noise immunity. MIL-STD-1553 is an ideal physical layer for use with TTP.

This report summarizes characterization testing that was performed on MIL-STD-1553 as a physical layer for Time Triggered Protocol (TTP). A 1553 physical layer board (1553 PHY) was developed by Data Device Corporation. The 1553 PHY was designed to be installed on a TTP development board (refer to Figure 1).

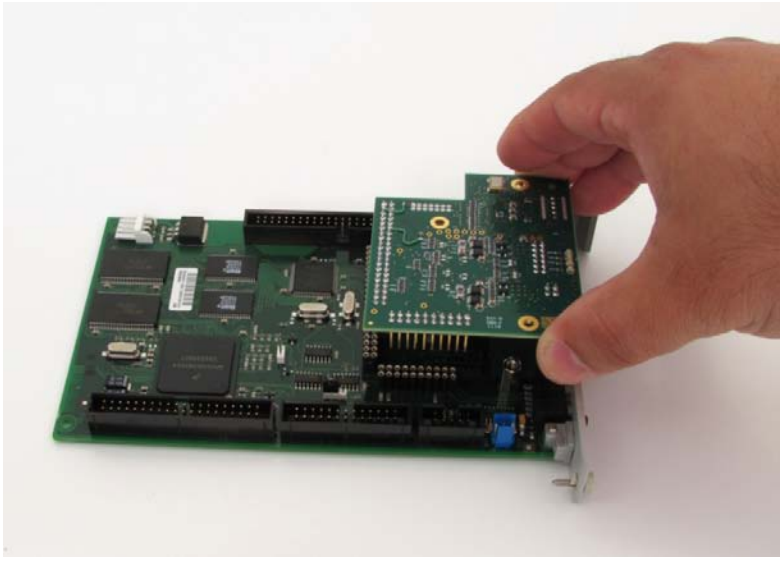


Figure 1. DDC's 1553 PHY Board for TTTech's Powernode TTP Controller Board

DDC's 1553 PHY board contains two MIL-STD-1553 transmitter/receivers (transceivers). The transceivers on the 1553 PHY board were designed to operate at data rates up to 5 Mbps. The TTP controller on the Powernode boards operates at 4 Mbps.

Test Equipment Used

Tektronix TDS5034B Oscilloscope
Tektronix P6246 Differential Probe
Tektronix 1103 TekProbe Power Supply
HP4396A Network / Spectrum Analyzer
HP85016A S-Parameter Test Set
Micronetics NOD-5107 Noise Source
Lambda LPT-7202-FM Power Supply
MIL-STD-1553 cables of various lengths
North Hills NH12826 MIL-STD-1553 Bus Couplers
North Hills 0101BB Baluns (50 ohm unb to 75 ohm bal)
Trompeter TNG-1-78 Terminators (78 ohm)
70 ohm Resistive Load
Kay Elemetrics Corp Model 432D Attenuator

Transmitter Characteristics

Setup

The setup for the 1553 PHY board transmitter measurements is shown in Figure 2. The 1553 PHY board contains DIP switches which can be used to enable test modes of operation. An external power supply was used to supply 5V and 3.3V to the 1553 PHY board. The DIP switches on 1553 PHY board were configured such that the board transmitted a fixed test pattern. The transmit test pattern consisted of a MIL-STD-1553 word that included a Sync plus 17 Manchester encoded bits at a data rate of 5 Mbps with a 25% transmit duty cycle. An oscilloscope was used to measure the output of the transmitter across a resistive load.

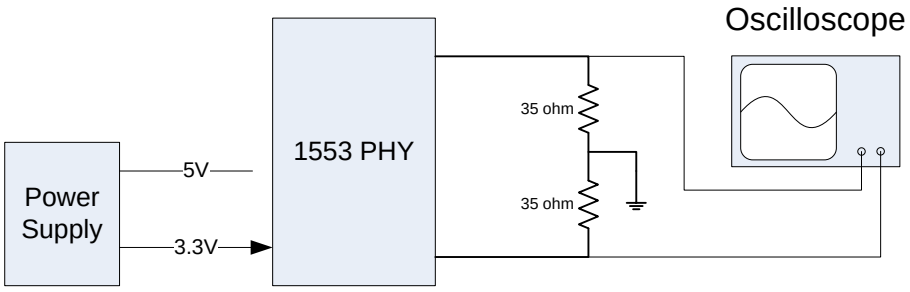


Figure 2. Transmitter Test Configuration

Measurements

Amplitude

MIL-STD-1553 specifies amplitude of the transmitter to be in the range of 18 to 27 V_{PP} across a 70 ohm resistive load. The amplitude of the 1553 PHY board was measured differentially across a 70 ohm resistive load. The transmit amplitude was 24 volts peak to peak (within the MIL-STD-1553 specification).

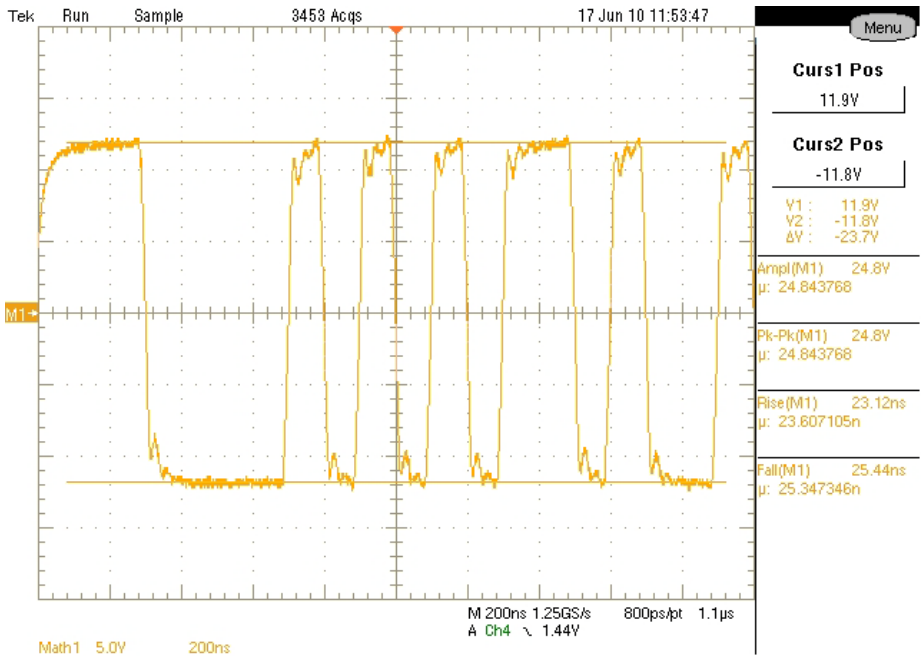


Figure 3. Transmit Waveform Showing Amplitude

Risetime/Falltime

MIL-STD-1553 specifies a transmitter to maintain a rise and fall time within the range of 100 to 300 ns for a 1 Mbps data rate. The 1553 PHY board is designed to run at 5 Mbps so the rise/fall time of the waveform needs to be scaled accordingly (i.e. 20 to 60 ns). The rise and fall time of the 1553 PHY board was measured to be 23 ns (refer to Figure 4).

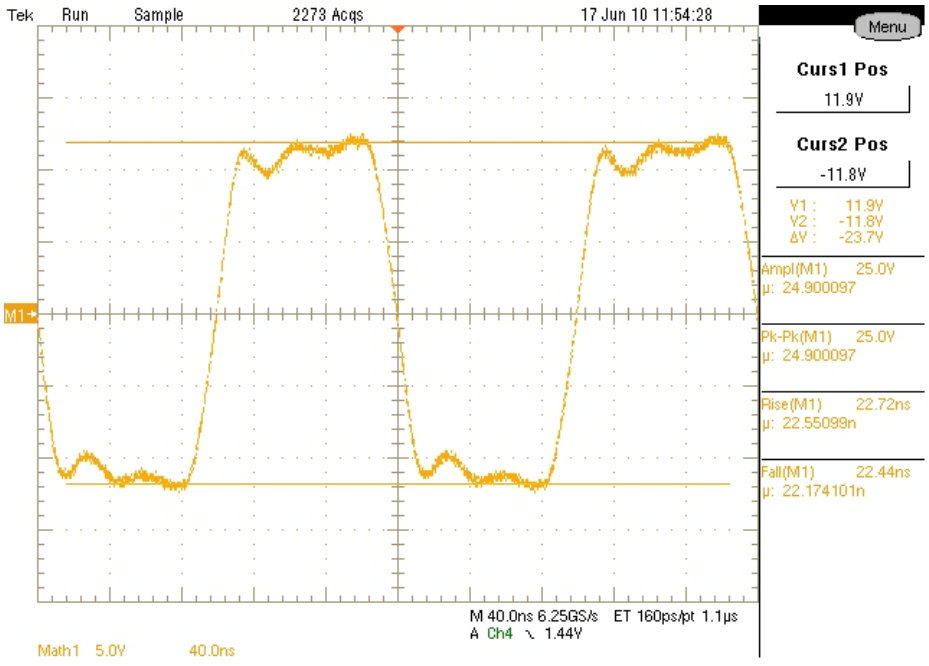


Figure 4. Transmit Waveform Showing Rise/Fall Time

Zero Crossing Stability

A Manchester line code produces a series a pulses in which the zero crossing points will be at multiples of the baud rate (i.e. multiples of 500 ns for 1 Mbps MIL-STD-1553). MIL-STD-1553 specifies that a transmitter must maintain a specific tolerance, referred as zero crossing stability, on the timing between subsequent transitions. The zero crossing tolerance for 1 Mbps MIL-STD-1553 is +/- 25 ns (5% of the baud time). The 1553 PHY board is designed to run at a Manchester coded data rate of 5 Mbps, which utilizes a 100 ns baud time. The proposed zero crossing stability for a 5 Mbps data rate is 5% of 100 ns or +/- 5 ns. Figure 5 shows the timing between consecutive zero crossings to be 98.96 ns, which is well within the proposed tolerance of 100ns +/- 5 ns. Note the zero crossing shown in Figure 5 is the first transition following the 1553 "sync" field. The large difference in frequency content between the sync pulse (consisting of pulse that is 3 baud times wide) and a data bit pulse (1 baud time wide) generally causes a large zero crossing error. In this case the zero crossing stability is well within spec.

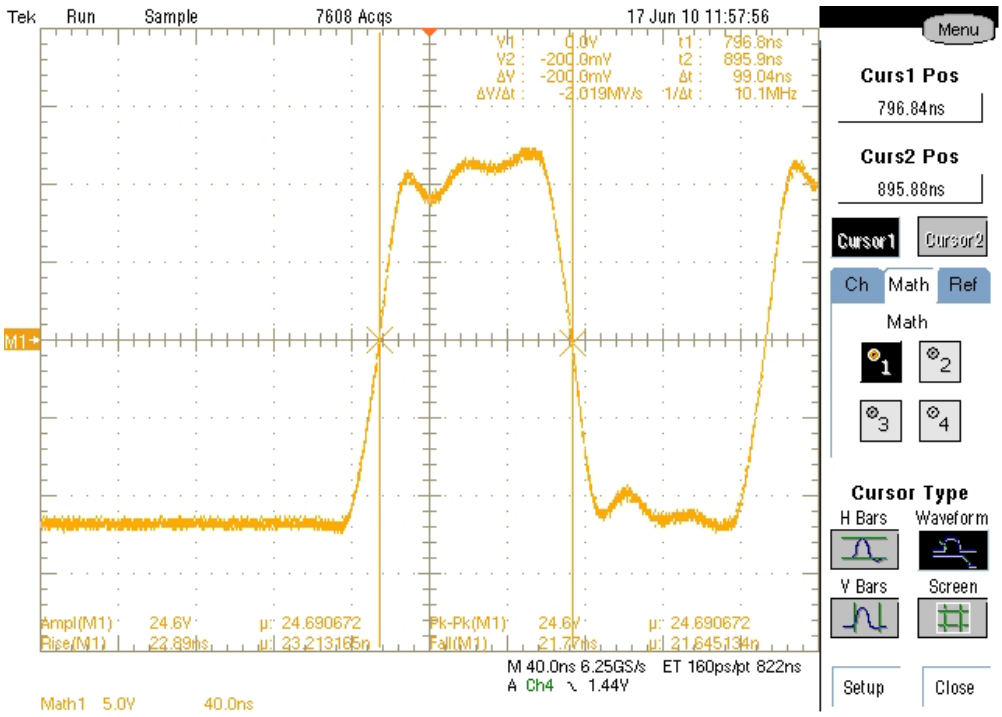


Figure 5. Zero Crossing Stability of 5 Mbps Manchester Coded Data

Analysis

A MIL-STD-1553 data bus will introduce both amplitude and phase distortion. Amplitude distortion will be in the form of attenuation while phase distortion will have the effect of changing the width of the transmitted pulses (i.e. shift the zero crossing points on the waveform). In order to bound the performance of the network it is necessary to specify both the transmitter and receiver with regards to amplitude and phase distortion. They two key transmit characteristics are amplitude and zero crossing tolerance.

Receiver Characteristics

Receiver Threshold

The receiver threshold on the 1553 PHY board was tested by plugging the 1553 PHY board into a test connector on a BU-65590F PMC card. The BU-65590F PMC card was loaded with custom FPGA firmware that would utilize transceivers on the 1553 PHY board and would implement MIL-STD-1553 protocol running at 5 Mbps.

Channel 1 on the BU-65590F PMC card was configured as a 1553 Bus Controller (BC) utilizing transceiver channel A on the 1553 PHY board while channel 2 on the PMC was configured as a Remote Terminal utilizing channel B on the 1553 PHY board. A pair of baluns and a programmable attenuator was used to decrease the amplitude of the BC signal to determine the receiver threshold of the RT (refer to Figure 6).

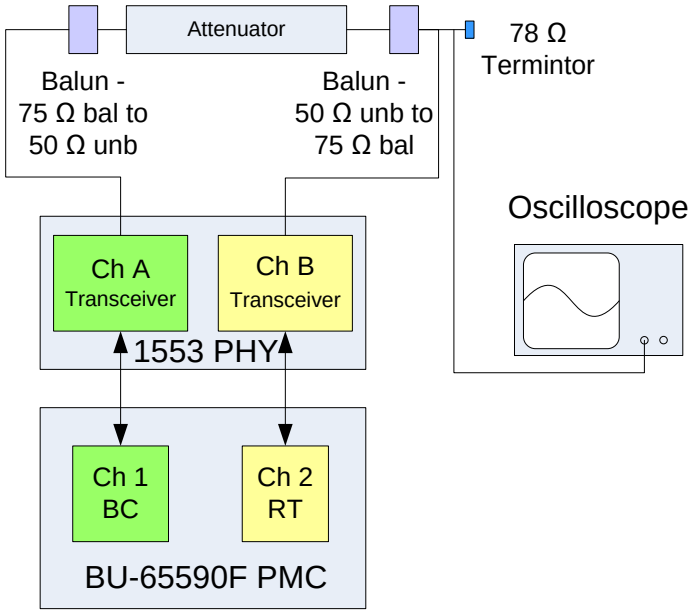


Figure 6. MIL-STD-1553 Receiver Threshold

The BU-65590F PMC and 1553 PHY boards were installed in a computer and custom software was written to run the BC and RT while displaying total message count along with an associated error count. The test was started with no attenuation (0 dB). The Bus Controller was setup to continuously send messages. The RT response was observed on the oscilloscope and was confirmed on the computer display (total messages increasing with zero errors). The attenuator was then used to decrease the amplitude of the BC signal until the RT stopped responding and the resulting signal level was measured on the oscilloscope (see Figure 7 for a sample waveform).

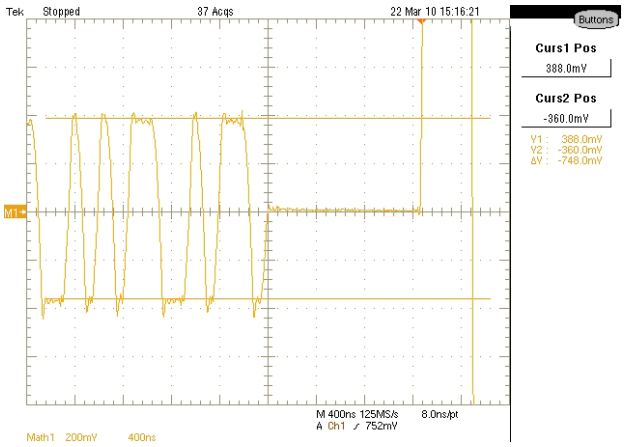


Figure 7. Attenuated BC Signal and RT Response

On channel A it was determined that the RT would not respond to a BC signal of 530 mV and would respond to a BC signal of 600 mV. On channel B the no response threshold was also 530 mV while the response threshold was 595 mV.

Receiver Filter Frequency Response

The frequency response of the receiver filter on the 1553 PHY board was characterized using an HP4396A Network Analyzer with an HP85016A S-Parameter Test Set (refer to Figure 8). A balun was connected to port 1 on the network analyzer. The purpose of the balun was to convert the unbalanced output from the network analyzer to a balanced signal and to convert the impedance from 50 ohms to 75 ohms. Port 2 on the network analyzer was connected to a receiver test point on the 1553 PHY board (i.e. the output of the receiver filter).

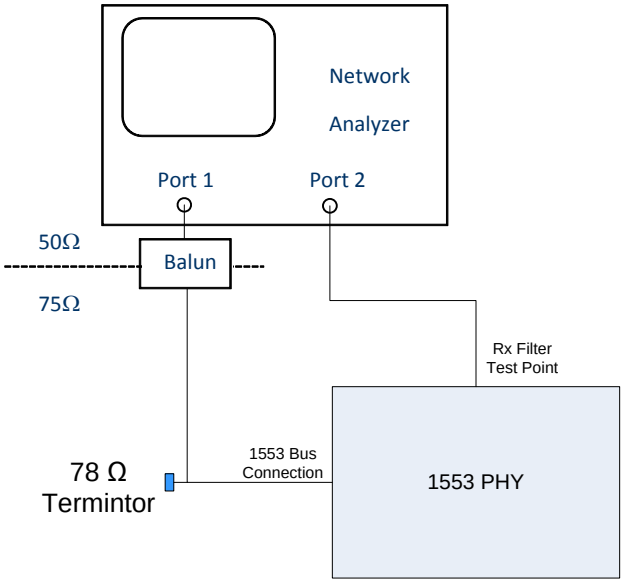


Figure 8. Receiver Filter Frequency Response Measurement

The network analyzer was programmed for a sweep frequency from 300 KHz to 20.3 MHz. The magnitude and group delay for the S21 (forward gain) are shown in Figure 9.

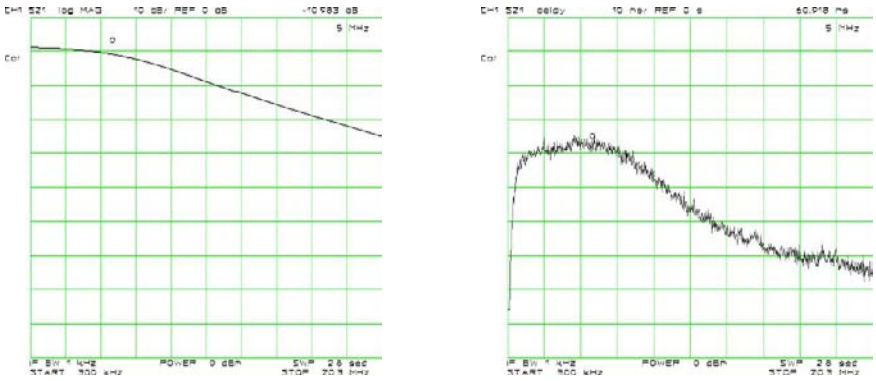


Figure 9. Gain Magnitude and Group Delay of Receiver Filter

Receiver Zero Crossing Distortion

A Manchester coded signal will consist of consecutive pulses with a width equal to the baud rate (500 ns for 1 Mbps 1553 and 100 ns for a 5 Mbps data rate). Phase distortion in the channel (i.e. on the bus) will have the effect of increasing or decreasing the width of each pulse (i.e. shifting the zero crossing point between consecutive transitions). The receiver needs to be designed to tolerate this phase distortion. MIL-STD-1553 specifies that a receiver must be able to decode a waveform with a zero crossing error of up to 150 ns (30% of the baud time) for a 1 Mbps data rate. The proposed limit for a 5 Mbps rate is 30% of 100 ns or 30 ns.

The zero crossing performance of a receiver is dependent on the combination of the analog receiver and the digital decoder. The analog receiver will convert the received signal into a series of digital pulses. The decoder will recover the embedded clock and convert the digital pulse stream into a serial data stream. The 1553 PHY board implements the analog receiver function while the TTP controller on the Powernode implements the decoder function.

Testing the receiver zero crossing distortion of a receiver requires specialized test equipment. For MIL-STD-1553 companies such as DDC provide MIL-STD-1553 test equipment that has the ability to transmit signals to a receiver under test with a programmable zero crossing error. It is our understanding that this type of equipment does not exist for TTP. TTP is also a more complicated protocol so it appears that a simple pattern generator cannot be used to test the receiver. A true test of the receiver will require a specialized tester that implements the TTP protocol.

The receiver filter characterization in the Receiver Filter Frequency Response section shows that the amplitude and group delay of the 1553 receiver is consistent over the proposed pass band, which implies that the receiver will not induce additional amplitude and phase distortion and thus the performance of the receiver in terms of tolerance to zero crossing distortion will be determined primarily by the digital decoder within the TTP controller. A more detailed understanding of the operation of the TTP controller will be required to assess the zero crossing performance of the decoder.

Analysis

The receiver threshold of the 1553 PHY is consistent with the values defined in MIL-STD-1553, thus the loss budget between a transmitted and received signal will be similar to that of MIL-STD-1553 (amplitude distortion). Although the receiver zero crossing distortion was not tested it is believed that the performance should be similar to 1 Mbps 1553. The analog receiver was shown to maintain the amplitude and phase of the received signal and the same decoder algorithm used in MIL-STD-1553 could be used with TTP (assuming that the decoder in the TTP controller is found to be deficient).

Network Characteristics

Setup

A test network was assembled consisting of a main bus length of 430 feet with 10 stub connections (refer to Figure 10). Each stub connection utilizes a standard MIL-STD-1553 bus coupler consisting of a coupling transformer and a pair of isolation resistors (as defined in MIL-STD-1553). Powernode cards with 1553 PHY boards installed on them (referred to as 1553 Powernodes) were connected to seven of the stubs on the bus. The other 3 stubs were terminated in a simulated load of 2000 ohms.

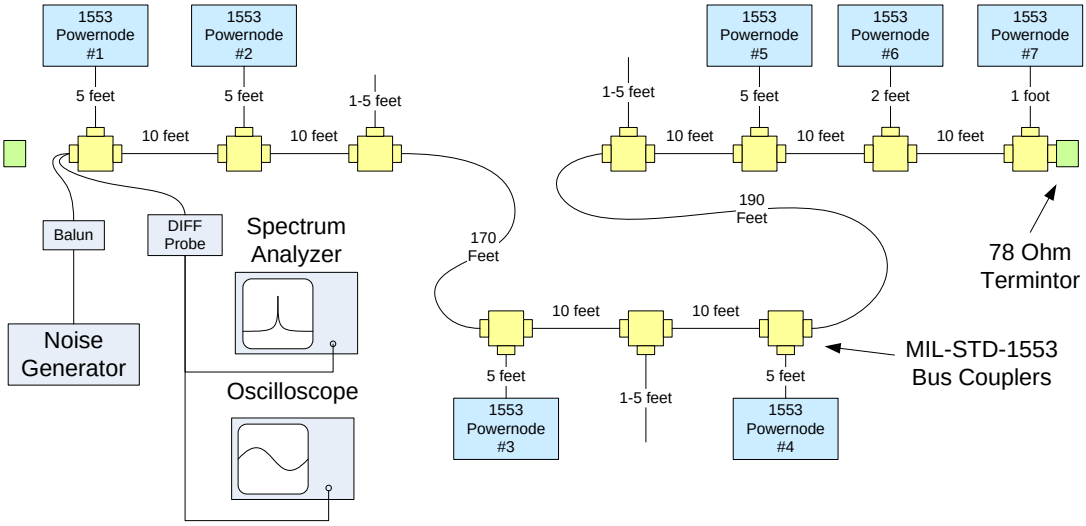


Figure 10. 430 Foot Test Bus

The terminator on one end of the bus (near 1553 Powernode #1) was removed and the end of the bus was connected to an NOD-5107 noise generator for bit error rate testing. A balun was used to convert the 50 ohm unbalanced output impedance of the noise generator to a 75 ohm balanced impedance (to match the 78 ohm impedance of the 1553 bus). The NOD-5107 outputs random noise from 100 Hz to 100 MHz with a maximum output power of -70 dBm/Hz.

Each 1553 Powernode contains custom firmware that implements a cluster cycle consisting of 2 rounds with a 4 ms cycle time. Each 1553 Powernode will send a 240 byte X-Frame in each of the two rounds (each X-Frame contains 16 bytes of TTP status

information such as the membership vector plus 224 bytes of actual data). The payload data consists of a cyclic pattern of 256 * 224 bytes of pseudo-random data (data is updated on each round). This firmware also displays bit error rate statistics on the console port every 10 minutes (total frame count along with error frame count and missing frame count). The TTP controller on the Powernode was configured to run at 4 Mbps. Note that the 1553 PHY board was designed to run at 5 Mbps but the Powernode firmware does not provide an option for running at 5 Mbps.

The network illustrated in Figure 10 was constructed to test multiple aspects of the bus including attenuation and phase distortion. The path from 1553 Powernode #1 to 1553 Powernode #7 is expected to provide the largest attenuation and the largest phase distortion due to dispersion (i.e. group delay of the channel). The path from 1553 Powernode #1 to Powernode #2 is expected to provide the smallest amount of attenuation, minimal dispersion and largest phase distortion due to reflections.

Eye Diagrams

The cluster was powered up and the waveforms were measured using the oscilloscope. Figure 11 shows an eye diagram measurement for Powernode #7 measured at the opposite end of the bus (as illustrated in Figure 10). The eye diagram clearly shows the difference in attenuation between 2 MHz and 4 MHz components of the Manchester waveform. The 2 MHz component of the waveform has been attenuated to 4.9 V_{PP} while the 4 MHz component has been attenuated to 3.3 or 2.8 V_{PP} (~ 4 to 5 dB difference). The amplitude of the received signal is well above the defined maximum defined receiver threshold of 1.2 V_{PP}.

The waveform in Figure 11 also shows jitter on the zero crossing points of the waveform. An ideal crossing will be in multiples of the baud time. A 4 Mbps Manchester line code consists of a series of 125 ns pulses so all the zero crossing points on the waveform should be multiples of 125 ns (baud time). MIL-STD-1553 defines that a receiver must tolerate a zero crossing error of up to +/- 30% of the baud time (i.e. +/- 150 ns for a 1 Mbps data rate). Scaling the receiver zero crossing tolerance to 4 Mbps yields a tolerance of +/- 37.5 ns. The received signal in Figure 11 contains a maximum zero crossing error of +12 ns (well within the proposed performance limit of +/- 37.5 ns).

The receiver threshold (1.2 V_{PP}) and zero crossing distortion (+/- 37.5 ns) specifications were used to form an eye mask, which is superimposed on the receive waveform in Figure 11.

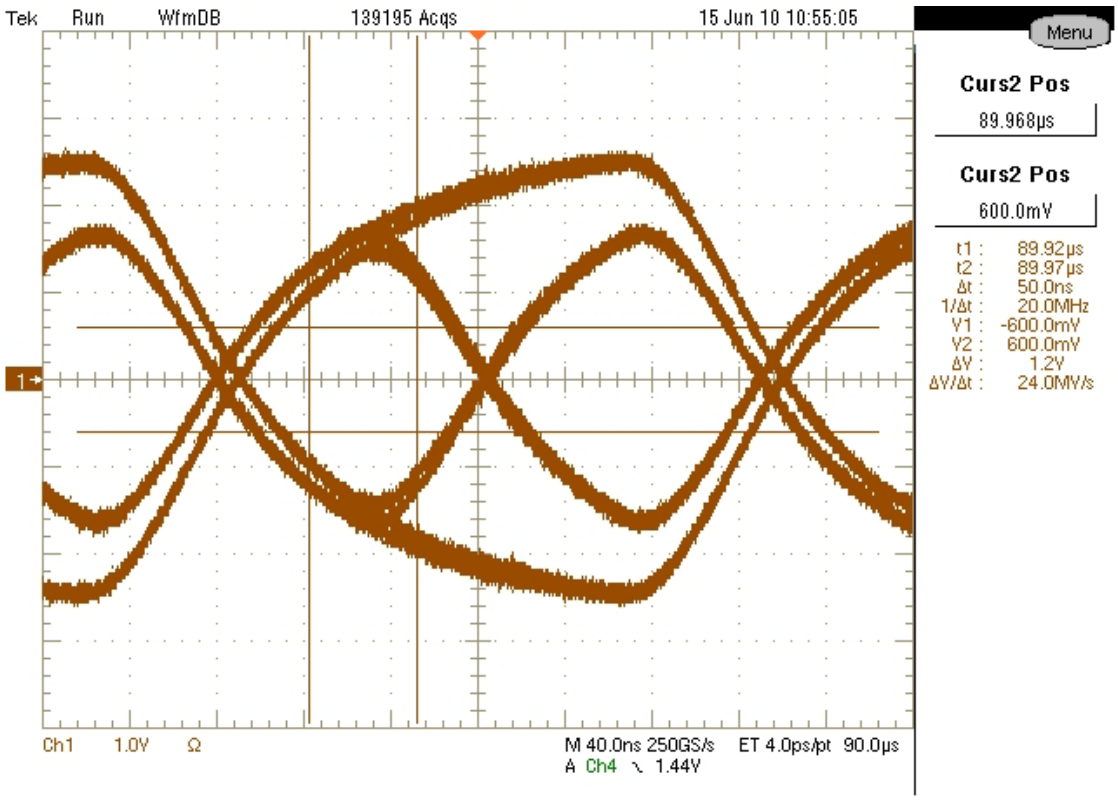


Figure 11. Eye Diagram for 1553 Powernode #7 on 430 Foot Bus with No Noise

Figure 12 shows an eye diagram measurement for 1553 Powernode #7 with the addition of -78 dBm/Hz of noise. This figure includes the same eye mask that was presented with Figure 11. This measurement shows that even in the presence of a very large noise source a stable eye pattern exists. The effectiveness of the eye mask will be substantiated later in this report when bit error rate testing is performed on this setup.

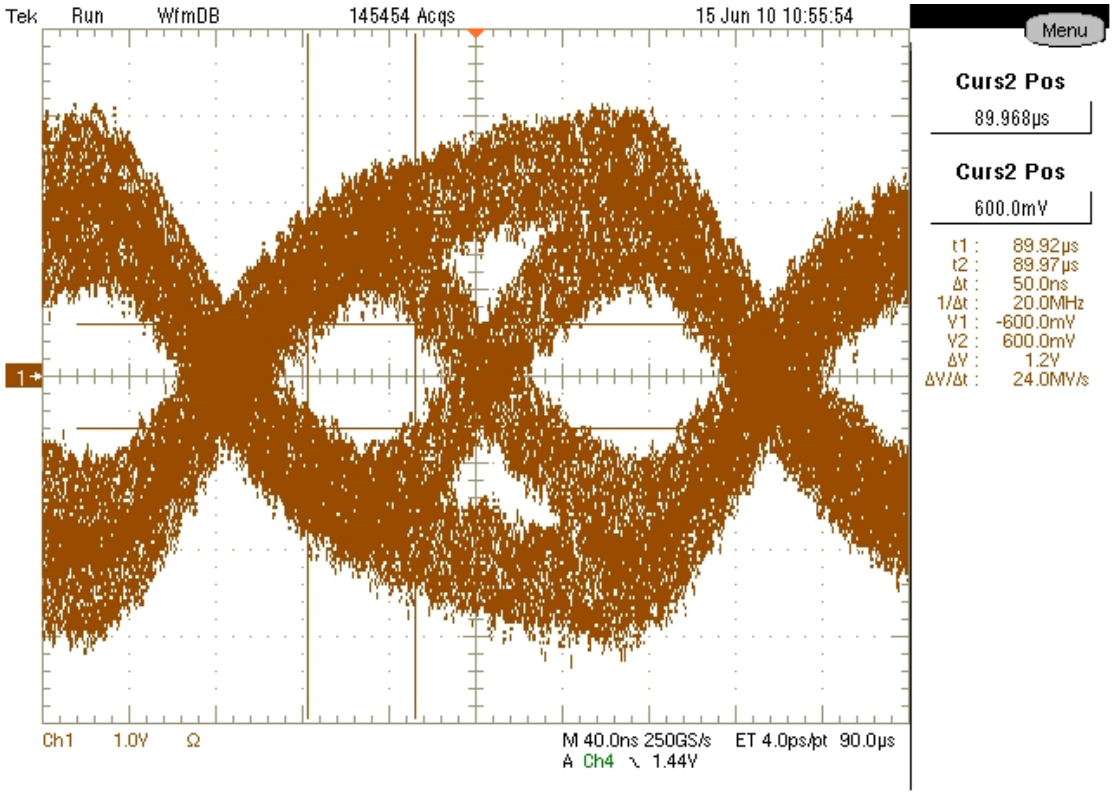


Figure 12. Eye Diagram for Powernode #7 on 430 Foot Bus with -78 dBm/Hz Noise

Insertion Loss Measurements

An HP4396A Network Analyzer with an HP85016A S-Parameter Test Set was used to measure the insertion loss through the bus from 1553 Powernode #7 to the other end of the bus (refer to Figure 13). Port 1 on the network analyzer was connected to the stub connection in place of 1553 Powernode #7 while port 2 was connected to the end of the bus (in place of one of the termination resistors. Baluns were used to convert the 50 ohm unbalance impedance of the network analyzer to a 75 ohm balanced impedance that is compatible with the characteristic impedance of the 1553 bus. The network analyzer was programmed for a sweep frequency from 300 KHz to 20.3 MHz.

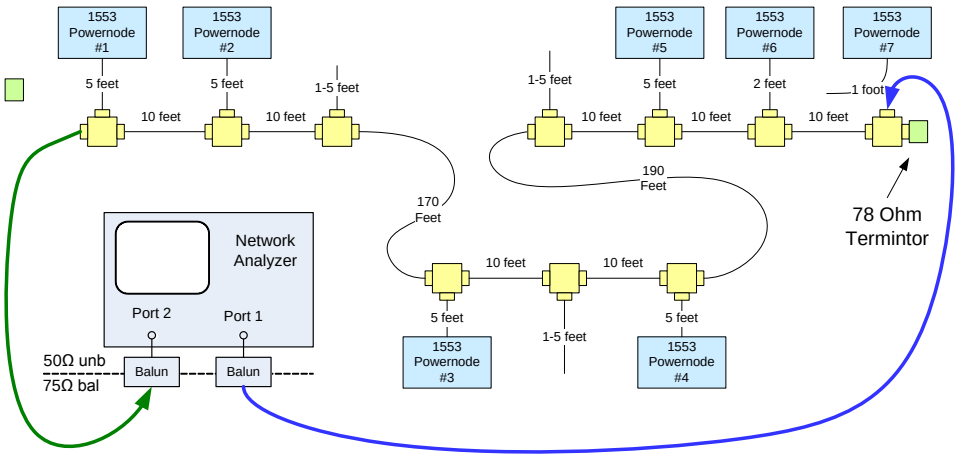


Figure 13. Insertion Loss Measurement Setup

Figure 13 illustrates the insertion loss measurement (i.e. the magnitude for the S21 forward gain) for the channel from the stub connection for 1553 Powernode #7 to the opposite end of the bus (on the bus near 1553 Powernode #1). The measurement shows the insertion loss to be -17 dB at 2 MHz and -21 dB at 4 MHz (a 4 dB difference). Note that this is fairly consistent with the voltage measurement in Figure 11 which shows a 4 to 5 dB difference between the 2 and 4 MHz Manchester pluses.

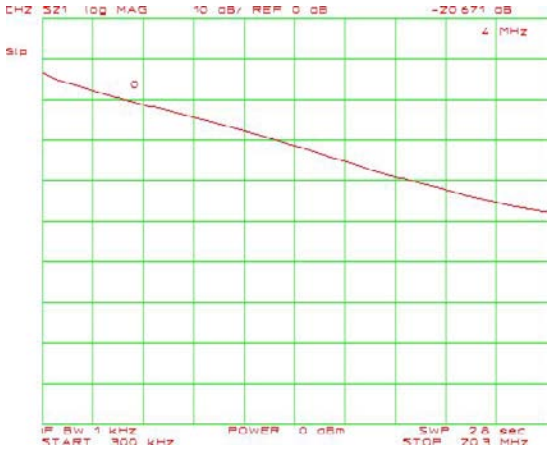


Figure 14. Insertion Loss from 1553 Powernode #7 to End of Bus

Bit Error Rate Measurements

Bit Error Rate (BER) testing was performed using the setup illustrated in Figure 10 (430 foot bus with 10 stubs). The console port on 1553 Powernode #1 was used to view the error rate statistics which are collected by the embedded processor on the Powernode card. The embedded processor displays total frames, error count, and missing frames every 10 minutes. Once the cluster is up and running the processor verifies the presence of a frame in every slot. If a frame is missing then the missing frame counter is incremented. If a frame is received with an error (i.e. a CRC failure) then the error counter is incremented.

BER testing was run with three different noise levels. The first test was run to calculate the BER of the network with nominal "laboratory" noise levels (external noise source turned off). The lab noise environment test was run over a long period of time (over 25 days) in order to achieve a high statistical confidence level in the BER. Additional testing was performed with higher noise levels to perform an "accelerated noise test". Note that MIL-STD-1553 also makes use of an accelerated noise test in order to be able to run BER testing in a reasonable amount of time. The power spectral density (PSD) of the noise used in the accelerated BER testing was -84 dBm/Hz and -78 dBm/Hz.

Figure 15 shows the spectrum analyzer measurements for both the receive signal (blue trace) and the injected noise (black trace). Note that 20 dB needs to added to the traces in Figure 15 to account for the use of a 10x scope probe. The measurement shows that the signal to noise ratio for this noise level (-78 dBm/Hz) is approximately 18 dB at 4 MHz. Note that an SNR of approximately 15.5 dB is required for a BER of 10^{-9}.(2)

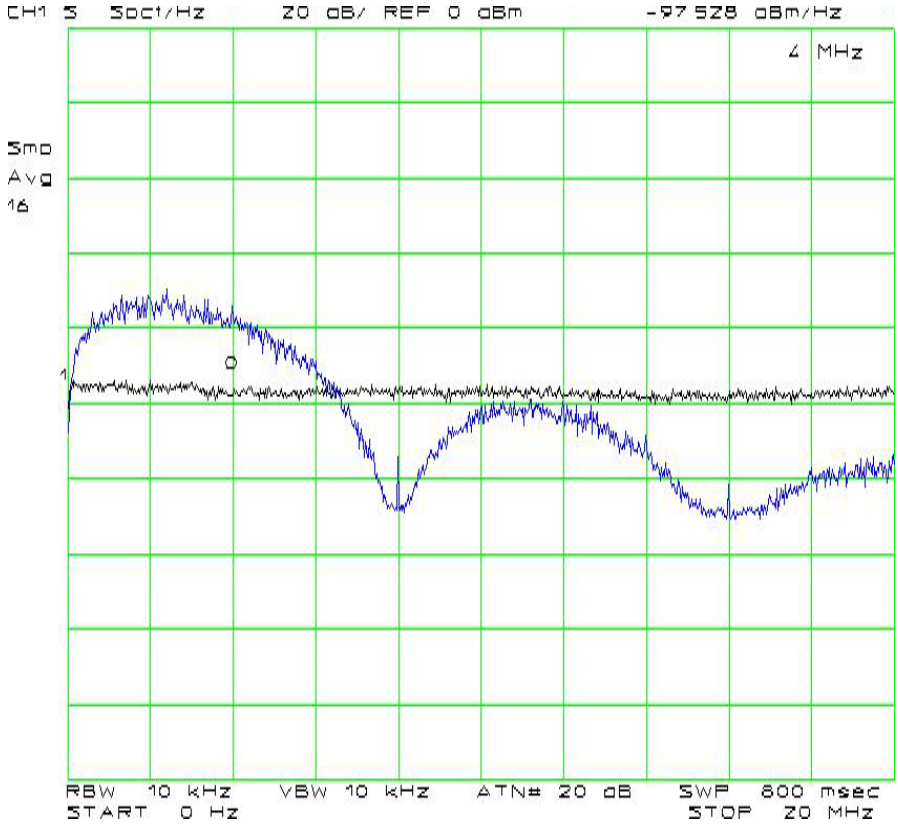


Figure 15. Spectrum Measurement of Receive Signal and Noise

The results of the BER testing, summarized in Table 1, represent the number of frames and associated bits that were received with zero errors. In addition the table provides a statistical confidence level for various bit error rates, based on the number of error free bits that were received.(3)

Table 1 - BER Test Results (with zero errors)

Noise Level (dBm/hz)	Total Frames	Total Bits	Time	Confidence Levels for Various Bit Error Rates			
				10^{-9}	10^{-10}	10^{-11}	10^{-12}
None	3.9×10^{9}	7.4×10^{12}	25.6d	100.0%	100.0%	100.0%	99.9%
-84	88.2×10^{6}	169×10^{9}	14h	100.0%	100.0%	81.6%	15.6%
-78	7.4×10^{6}	14.1×10^{9}	1.2h	100.0%	75.6%	13.2%	1.4%

Analysis

The test configuration used in sections 5.2 through 5.4 was constructed to provide a test bed that represents a demanding data bus configuration. The eye diagram measurements showed that the receiver contains significant margin. An eye mask was constructed based on the defined receiver characteristics. The eye mask predicted that the receive signal with a high noise level shown in Figure 12 had significant margin

that the receiver should be able to decode the waveform. The BER testing in section 5.4 confirmed the eye mask by showing that the BER for the configuration was less than 10^{-9}.

Phase distortion was kept to a minimum on the network (12 ns of zero crossing error for 125 ns pulses). The low phase distortion is attributed to the use of bus couplers as defined in MIL-STD-1553. Bus couplers have the effect of matching the impedance of the stub looking into the bus and increasing the effective impedance presented by the stub connection to the bus which results in a lower reflection coefficient and thus less phase distortion on the bus.(4)

Noise testing was performed with power levels that are far above those expected to be present in an aircraft environment. Past measurements conducted by DDC on an F-15 aircraft showed the PSD of background noise on a real MIL-STD-1553 bus to be approximately -120 dBm/Hz, which is significantly lower than the noise levels used in the accelerated BER testing.(5) The 1553 Powernodes showed superior BER performance even in the presence of abnormally high noise.

Conclusion

Testing has shown that 4 Mbps TTP utilizing a 1553 PHY provides robust performance while maintaining the key architectural benefits of MIL-STD-153 including galvanic isolation. Interoperability was shown between a commercially available TTP controller and a 1553 PHY. This technology demonstration establishes a performance baseline for TTP 1553 and highlights the robust performance that makes it an ideal solution for demanding applications such as commercial aircraft systems.

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2. **Proakis, John G.** *Digital Communications Fourth Edition.* s.l. : The McGraw - Hill Companies, Inc., 2001.

3. **Redd, Justin.** Calculating statistical confidence levels for error-probability estimates. *Lightwave Magazine.* April, 2000.

4. *MIL-STD-1553 – A Robust Data Bus For Commercial Aircraft.* **Hegarty, Michael.** Farmingdale : IEEE, 2010. Long Island Systems, Applications and Technology Conference.

5. *High Performance 1553 F-15E Mux Bus Capacity Study Prepared for the Boeing Compnay.* **Data Device Corporation.** Bohemia : s.n., 2004.

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Data Device Corporation is recognized as an international leading supplier of high-reliability data interface products for military and commercial aerospace applications since 1964 and MIL-STD-1553 products for more than 25 years. DDC's design and manufacturing facility is located in Bohemia, N.Y.

SECTION 3:

1553 EVOLUTION WHITE PAPER

MIL-STD-1553 Evolves with the Times

Introduction

MIL-STD-1553 is a serial, time division multiplex data bus that has been used as the primary command and control data interconnect in military aircraft for the past three decades. MIL-STD-1553's robust performance, high level of interoperability, large installed based, and well established infrastructure of vendors has made MIL-STD-1553 the network of choice for military avionics systems.

The use of MIL-STD-1553 is not limited to military aircraft. MIL-STD-1553's use is pervasive in military ground vehicles, military ships, and satellite systems. All of these applications share common requirements for a deterministic, fault tolerant data bus that will operate in relatively harsh environments.

New Applications

Even after 30 years MIL-STD-1553 is finding its way into new applications. Airbus has selected MIL-STD-1553 for use in the flight control system for the A350 XWB aircraft (1).

MIL-STD-1553 combines a robust physical layer with a deterministic protocol making it ideally suited for use in commercial aerospace systems. In particular the galvanic isolation provided by transformers contributes to the superior EMI and lightning immunity of MIL-STD-1553. Isolation is even more critical in new composite aircraft where the skin of the aircraft no long provides an inherent Faraday shield as was the case with aluminum skinned aircraft.

One of the misnomers about MIL-STD-1553 is the perception that it is an expensive interface. The reality is that the cost of implementation of MIL-STD-1553 has decreased significantly over the last 10 years. There exists a mature ecosystem of MIL-STD-1553 suppliers that provide cost effective solutions for embedded controllers, cable harnesses, test and simulation equipment, and software tools. Why invent a new interface when there is one available that has over 30 years of flight experience.

Higher Data Rates

While MIL-STD-1553's 1 megabit-per-second data rate is still adequate for a large number of applications, there are systems that require higher rates. Two approaches to increasing the bandwidth of MIL-STD-1553 are gaining momentum. The first approach, referred to as "Turbo 1553", is to simply increase data rate without changing any of 1553's architectural features (modulation technique, line code, coupling methods, etc). The second approach, referred to as "High Performance 1553" or "HyPer-1553", is to implement a high frequency broadband waveform using alternate line codes and modulation methods. The second approach can also be extended such that it can coexist with traditional 1 Mbps 1553 on the same wire through the use of frequency division multiplexing.

Turbo 1553 – An Evolutionary Approach

MIL-STD-1553 has a well established set of design guidelines for a network operating at 1 M bps. In addition to over thirty years of in service history there is a strong analytical foundation for these guidelines which is well documented in MIL-HDBK-1553A. (2) The key design variables in a 1553 network are bus length, number of stubs, location of stubs, and length of the stubs. The concepts defined in the standard and the handbook can be extended to data rates above 1 Mbps. The question becomes what impact would a higher data rate have on these design variables and the resulting performance of the network.

The first step towards an implementation of Turbo 1553 is to understand the impact of higher frequency on a ttenuation and phase distortion. Attenuation impacts the amplitude of the signal that is presented to the receiver, and as such impacts the resulting signal to noise ratio (SNR). SNR is a key benchmark in defining the throughput capacity and bit error rate (BER) of a network. Phase distortion, also referred to as jitter or zero crossing error, impacts the relative timing of pulses which in turn can lead to problems with inter-symbol interference which also has an impact on the bit error rate of the receiver.

Attenuation

Attenuation occurs due to the resistance, series inductance and shunt capacitance of the cables. The attenuation will include both a frequency independent component due to the resistance of the cable and a frequency dependent component due to the parasitic capacitance and inductance. The cable can be approximated as a low pass filter.

MIL-STD-1553 provisions for approximately 12.6 dB of signal loss in the bus cable, based on a minimum transmitter voltage of 6 v olts and a minimum stub voltage requirement of 1.4 V (both measured peak to peak on the bus). MIL-STD-1553 defines the minimum stub voltage to be 1.3 dB above the terminal's maximum receiver threshold. Figure 1 illustrates the frequency response of 300 feet of MIL-STD-1553 cable from 300 KHz to 10 MHz. The attenuation through 300 feet of cable is -2 dB at 1 MHz and -5 dB at 5 MHz, both of which are well within the 12.6 dB link budget defined in MIL-STD-1553.

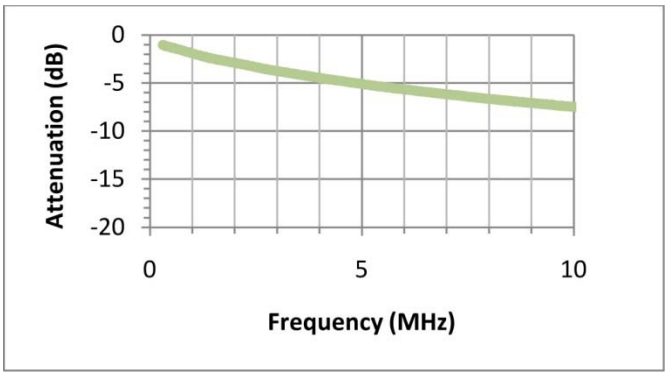

Figure 1. Frequency Response of 300 Feet of 1553 Cable

The signal attenuation will also be affected by the number of stub connections on the bus. Figure 2 illustrates the frequency response of a 460 foot bus with 10 stubs versus

460 of cable with no stub connections. At higher frequencies the attenuation will be influenced more by the presence of stubs connections.

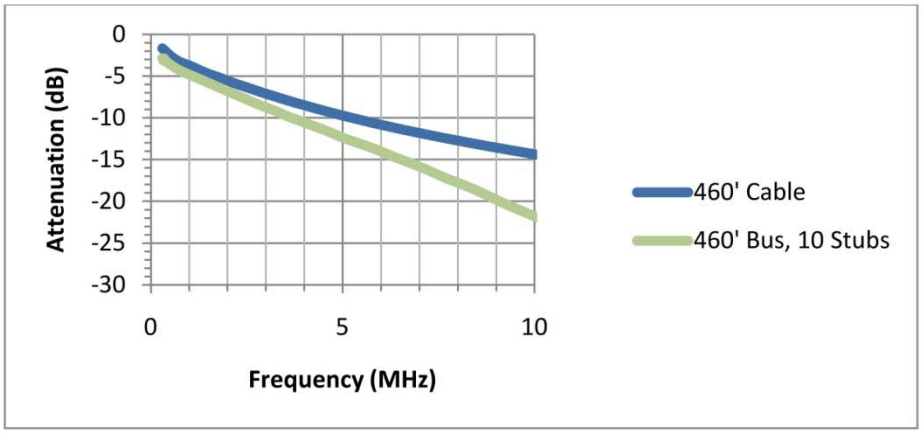

Figure 2. Insertion Loss of 460' Cable and 460' Bus from 300 KHz to 20.3 MHz

Phase Distortion

Phase distortion on a 1553 bus is primarily caused by two mechanisms: reflections. Dispersion is caused by variations in propagation velocity as a function of frequency. The amount of dispersion is determined by the characteristics of the cable (such as distributed capacitance). Reflections are caused by a mismatch in impedance on the transmission line due to stub connections. The impedance discontinuity at each stub connection will be based on the parallel combination of the stub impedance and the characteristic impedance of the main bus. As illustrated in Figure 3, a mismatch in impedance will split an incident wave into three components: a reflected wave, a transmitted wave, and a stub wave.

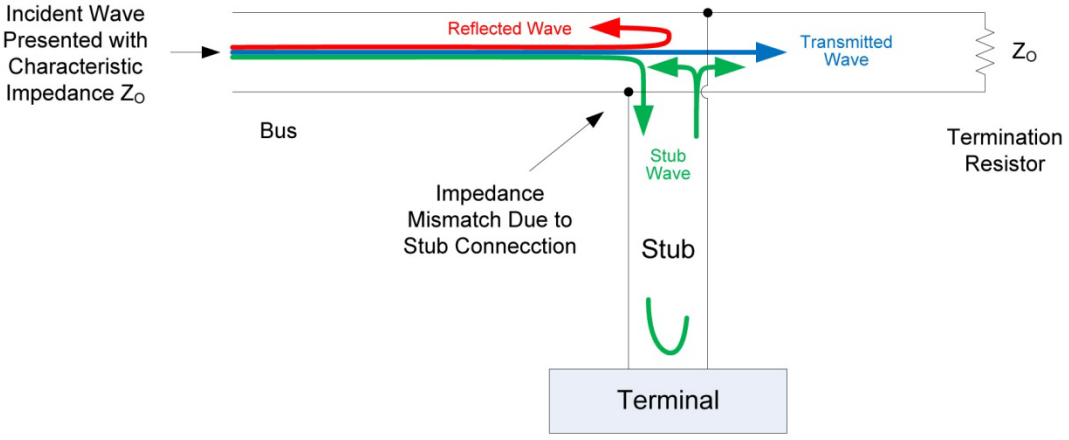

Figure 3. Reflections Caused by Impedance Mismatch

MIL-STD-1553 defines a terminal (communication end point) to have a high input impedance relative to the characteristic impedance, which will produce a large reflection coefficient at the boundary between the end of the stub cable and the

terminal. The implication of this high reflection coefficient is that most of the energy in the "stub wave" will be reflected back towards the main bus. The reflected stub wave will add back into the incident wave with a phase shift due to the round trip delay down the stub cable and back. The benefit of the reflected stub wave is that it minimizes attenuation but this is accomplished at the expense of a slight phase distortion. As long as the length of the stub is kept reasonably short the phase distortion induced by the stub wave will be minimal.

A lower stub impedance will result in a higher reflection coefficient on the main bus. The impedance of the stub will be based on the input impedance of the terminal as seen through the stub cable. Figure 4 illustrates the effective stub impedance as a function of stub length. As the stub length is increased the effective impedance of the stub decreases dramatically, which will result in an increase in reflections on the main bus. Figure 4 shows that a direct coupled connection to a 1553 bus with a 20 foot stub cable will result in approximately the same effective stub impedance for a terminal with a 1000 ohm input impedance as with a terminal with a 2000 ohm input impedance.

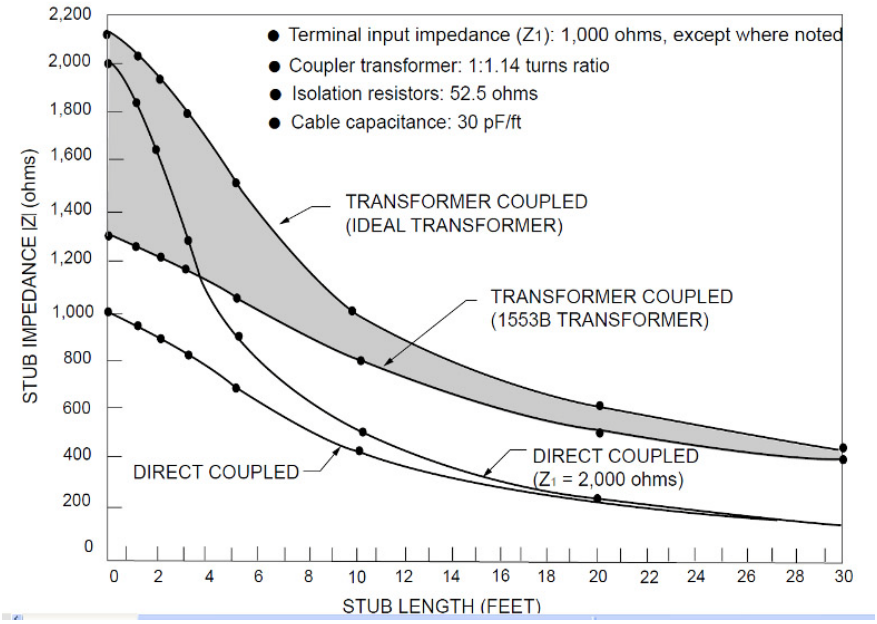

Figure 4. Stub Impedance Versus Stub Length

MIL-STD-1553 provides a second method for connecting to the main bus called transformer coupling. A transformer coupled connection utilizes an impedance matching coupling transformer along with isolation resistor to make the connection to the bus. The effect of the coupling transformer and isolation resistors is that the impedance of the stub looking into the bus is matched to the characteristic impedance. Providing a matched impedance looking into the bus will reduce secondary reflections on the stub and deliver the majority of the signal power to the bus. The second benefit of the coupling transformer is that the ratio is such that the effective stub impedance will be increased by a factor of 2 to 1 (based on the usage of a transformer with a turns ratio of 1.41:1). Figure 4 shows a significant increase in effective stub impedance for transformer coupled connections as compared to direct coupled connections. This use of bus couplers is one of the key architectural advantages of MIL-STD-1553 in terms of maintaining the fidelity of the transmission line on a multi-drop bus.

On long buses dispersion will contribute to the phase distortion in addition to reflections. The series resistance, parallel capacitance, and series inductance of the cable produce a non-linear phase response which will lead to a non-uniform group delay. Simply stated signals at different frequencies will take different amounts of time to propagate down the bus. In general, high frequency pulses propagate faster than lower frequency pulses.

A Manchester line code will utilize pulses at two primary frequencies (one at the baud rate and one at half the baud rate). A non-uniform group delay can result in intersymbol interference. Intersymbol interference occurs when a pulse in one symbol is delayed relative to a pulse in the next symbol. The result of intersymbol interference is a shift in the timing of subsequent edges in the waveform. This causes problems because the receiver uses the relative timing of the waveform transitions to recover the digital encoded data.

The amount of dispersion that occurs is a function of the frequency response of the cable and the length of the cable. MIL-STD-1553 defines the use of cable with reasonably good frequency response which allows for relatively long buses (100 meters and longer). Longer buses are also possible but care needs to taken in selecting the cable. A lower capacitance cable will produce lower attenuation and lower dispersion.

Test Results for Turbo 1553

Testing was performed on MIL-STD-1553 terminals operating at 4 Mbps (as compared to 1 Mbps). The result of the testing is that MIL-STD-1553 will operate reliably at 4 Mbps with excess margin. Figure 1 illustrates the test network that was used to evaluate MIL-STD-1553 running at higher speed. Various length stubs were used ranging in length from 1 foot to 5 feet. The length of the test network was 430 feet with 10 stub connections. The bus controller was implemented within terminal #1.

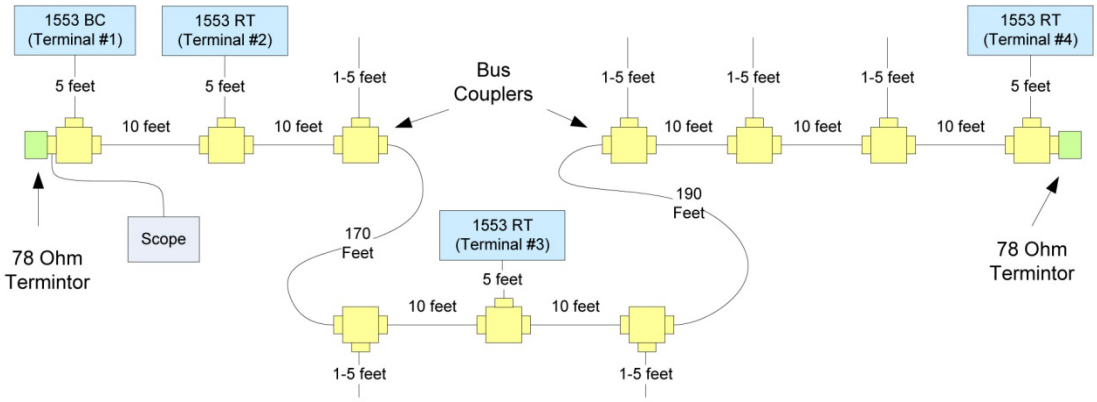

Figure 5. MIL-STD-1553 Test Network

Communication was tested between the Bus Controller (terminal #1) and three other terminals (1553 Remote Terminals). Terminal #2 is positioned to provide the least amount of attenuation but the largest amount of phase distortion due to the reflections. Terminal #3 provides a moderate amount of attenuation and phase distortion due to reflections. Terminal #4 was intended to provide the most attenuation and the largest phase distortion due to dispersion.

The bus controller was able to reliably communication with the three remote terminals. Scope measurements were made to measure the attenuation and phase distortion of signals from all three remote terminals. The result of the testing is that the waveforms are all well within the specified receiver specifications.

High Performance 1553 – A Revolutionary Approach

High Performance 1553 is a new technology that provides higher data rate communication over MIL-STD-1553 cabling. High Performance 1553 seeks to satisfy two goals: to enable high speed communication on a multi-drop bus, and to implement that communication such that it does not interfere with legacy 1 Mbps communication.

Technology

The data rate of a high performance 1553 system will be determined by the signal to noise ratio of the HyPer-1553 signal. DDC has conducted studies to determine the capacity of MIL-STD-1553 networks based on a prediction of the achievable signal to noise ratio. These studies take into account the signal loss of various bus configurations, EMI constraints (radiated emissions), and the expected noise environment. These studies have shown that there is sufficient bandwidth to implement a broadband system in which legacy 1 Mbps signals can coexist with new high speed signals supporting data rates up to 200 Mbps depending on the length of the bus and number of stubs. (3)

Multi-Drop Bus

A multi-drop bus has been viewed as the most cost effective topology for "low speed" networks because it eliminates the need for active hubs or switches. Implementation of a multi-drop bus becomes more difficult for data rates above 5 to 10 Mbps because of signal distortion. Realizations of "high speed networks" (such as Gigabit Ethernet) generally utilize point to point links with an active switched fabric, which avoids the challenges of a multi-drop bus but adds both cost and complexity to the system. The reality is that with the right technology a more efficient network can be implemented using a multi-drop bus.

HyPer-1553 combines the benefits of a multi-drop drop bus (reduced size, weight, power, and cost) with high data rates that have been historically restricted to a switched topology. The benefits of a multi-drop become even more dramatic in high assurance applications, such as commercial aircraft. In addition to the recurring manufacturing cost, an active switch will have very high development and qualification costs especially when you start to consider the implications of redundancy.

There is a gap between the low speed and high speed networks that is not effectively served by currently available COTS technology. High Performance 1553 is aimed at supplying a solution for "middle speed networks" with a data rate in the rage of 10 to 100 Mbps. High Performance 1553 provides reliable high speed communication on a multi-drop bus through the use of advanced signaling and filtering techniques.

Concurrent Operations

A key benefit of High Performance 1553 is the ability to extend the capabilities of existing systems that utilize MIL-STD-1553. High Performance 1553 provides these systems with the ability to add higher data rate communication without interfering with

the operation of the reliable 1 Mbps MIL-STD-1553 interface. The fact that traditional MIL-STD-1553 and high speed HyPer-1553 share the same cable contributes to significant weight reduction, especially when you compare HyPer-1553 to other high speed solutions that require hubs and/or switches.

High Performance 1553 utilizes frequency division multiplexing to allow concurrent high speed and low speed communication. The Traditional 1 Mbps MIL-STD-1553 signal occupies the lower portion of the frequency spectrum, while the new high speed signal utilizes a frequency band above traditional MIL-STD-1553 (refer to Figure 6). The resulting signal to noise ratio will be dependent on the frequency band that is selected for the high performance 1553 waveform.

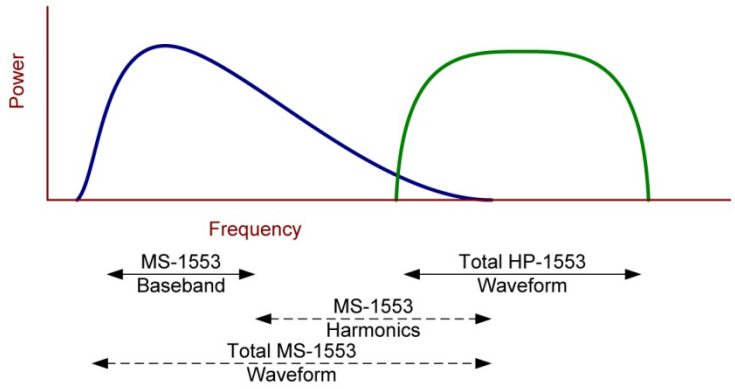

Figure 6. Frequency Spectrum

A legacy MIL-STD-1553 baseband signal (MS-1553) consists of four fundamental frequencies (250 KHz, 333 KHz, 500 KHz, and 1 MHz) plus harmonics. The frequency band of the high performance 1553 (HyPer-1553) waveform must be high enough to avoid the harmonics from the legacy MS-1553 signal. These MS-1553 harmonics will add to the noise presented to a HyPer-1553 receiver, thus reducing the signal to noise ratio and limiting the achievable data rate.

The upper bound of the HyPer-1553 frequency band will be constrained by signal loss through the 1553 cabling. Signal attenuation and distortion both increase as a function of frequency. Above a certain frequency a transmitted waveform will be attenuated to an extent that the receiver cannot differentiate the signal from noise (i.e. the signal to noise ratio becomes too low or negative).

The transmit level of the HyPer-1553 waveform is limited by the requirement to control the emission of radio frequency energy (RF emissions). Radiated emission levels are defined in MIL-STD-461 (applicable to military applications) and DO-160 (applicable to commercial aircraft).

The new high performance 1553 (HyPer-1553) waveform is implemented as a band limited signal such that it will not interfere with the lower frequency MIL-STD-1553 waveform (MS-1553). To a legacy MIL-STD-1553 terminal the HyPer-1553 signal appears as high frequency noise that will be filtered out by its receiver.

Future Upgrade Path

A common requirement driving system architectures is a desire to provision for future expansion. For data networks this implies that a portion of the communication bandwidth be reserved for additional capabilities that may be added in the future. HyPer-1553 provides the unique ability to implement a 1 Mbps bus today and then implement a much higher speed interface in the future utilizing the same cabling. This allows system architects to utilize a more cost effective 1 Mbps bus today without sacrificing future bandwidth availability.

Not Just a Concept

DDC successfully demonstrated an implementation of High Performance 1553 technology in a 2 hour flight onboard a USAF F15-E1 Strike Eagle fighter in December 2005. (4) HyPer-1553 was used to transfer imagery between a rugged computer mounted in the forward avionics bay and a smart bomb mounted on wing pylon station. The imagery data was transferred error free at 40 Mbps over existing 1553 cabling concurrently with legacy 1 Mbps transfers. The flight demonstration showed the viability of high speed communication on a multi-drop bus in harsh environments and the viability of concurrent operation with 1 Mbps 1553.

Figure 7. F-15E1 Taking off for HyPer-1553 Flight Demonstration

Adapting Commercial Technologies

It is very common for military/aerospace systems to make use of automotive components. Some of the environmental requirements are similar and the production volumes associated with automotive applications lead to relatively inexpensive chips. The challenge facing mil/aero systems designers is adapting these automotive chips to meet the specific requirements of aerospace applications in a cost effective manner.

FlexRay is an automotive communication system that appears to be appealing for use in aerospace applications. There are several manufacturers of embedded microcontroller chips with integrated FlexRay interfaces. FlexRay, which provides a 10 Mbps deterministic interface, would appear to be a strong candidate for use in real-time aerospace control systems except for the limitations of its physical layer.

FlexRay's physical layer is optimized for use in automotive applications which make use of low cost unshielded cables. The transmit signal level is constrained to a very low level in order to meet automotive emission requirements. The physical layer provides

robust communication in automotive applications where distances are relatively short (less than 24m), however studies have shown that the physical layer of FlexRay is inadequate for use in aerospace applications where cable distances may exceed 100m. (5)

Time Triggered Protocol (TTP) is another example of a commercial communication interface that may be considered for use in aerospace applications. TTP defines a robust, deterministic protocol but does not define a physical layer. RS-485 has been the de facto standard physical layer for use with TTP in commercial applications but studies have shown that the performance of RS-485 to be unreliable for use in aerospace applications due to RS-485's low transmit level and loosely defined receiver characteristics. (6)

Both FlexRay and TTP suffer from weaknesses in their physical layers when considering them for use in aerospace applications. MIL-STD-1553 can be used as an enabling technology for extending the use of these commercial data buses into aerospace applications. MIL-STD-1553's existing 1 Mbps physical layer combined with the higher speed derivatives described above provide an ideal framework for adapting commercial communication interfaces for use in harsh aerospace environments. Combining commercial communication controllers with robust MIL-STD-1553 PHYs provides the best of both worlds. System designers can leverage economies of scale associated with commercial controller chips and still satisfy the challenging physical layer and harsh environmental requirements of aerospace applications.

TTP 1553 Test Results

DDC has demonstrated a communication system utilizing commercially available TTP controllers combined with MIL-STD-1553 physical layer transceivers running at 4 Mbps on a 430 foot bus with 10 stub connections (refer to Figure 8). The network was characterized for attenuation and phase distortion at various stubs. Eye diagram measurements were made, and bit error rate testing was performed.

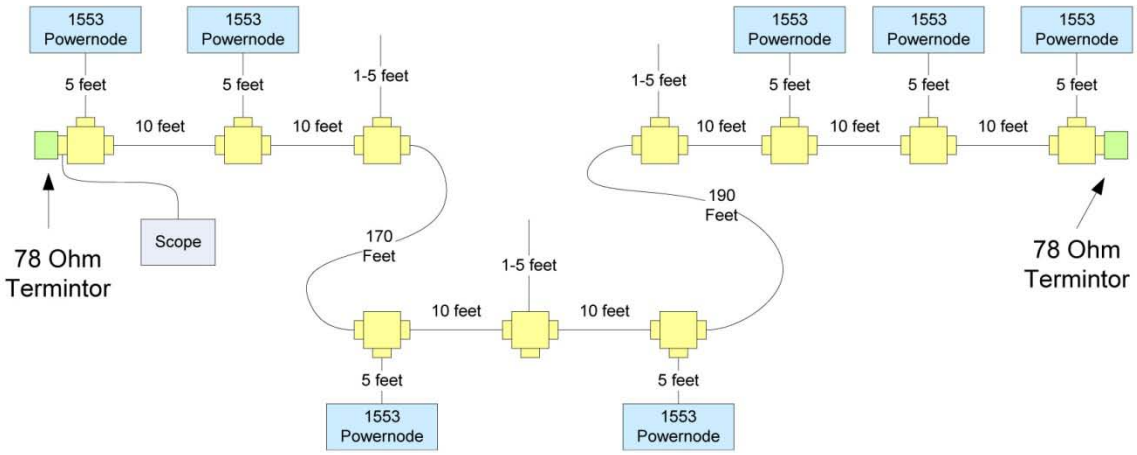

Figure 8. TTP 1553 Test Network

The results of the testing showed that MIL-STD-1553 can be utilized to provide TTP with a robust physical layer that is appropriate for even the most demanding aerospace applications such as flight control.

Summary of Solutions

Solution	Data Rate	Application	Concurrent 1 Mbps 1553
MIL-STD-1553	1 Mbps	Reliable, real-time, deterministic multi-drop bus	N/A
Turbo-1553	5 Mbps	New systems that require slightly higher data rates than 1 Mbps	No
HyPer-1553	50 to 100+ Mbps	New systems that require higher data on a multi-drop bus	No
HyPer-1553	10 to 50 Mbps	Incremental updates to systems already using 1 Mbps 1553	Yes

Conclusion

MIL-STD-1553's robust physical layer combined with emerging high speed derivatives serve as an ideal set of building blocks for a variety of applications. The superior isolation performance of MIL-STD-1553 makes it an extremely attractive solution for applications with severe EMI and lightning environments such as commercial aircraft. In addition the decades of in service flight history supports the notion that MIL-STD-1553 is well suited for critical real-time systems such as flight controls. The use of MIL-STD-1553 on the A350 aircraft is a testament to 1553's effectiveness for use in real-time, high assurance systems (1).

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Data Device Corporation is recognized as an international leading supplier of high-reliability data interface products for military and commercial aerospace applications since 1964 and MIL-STD-1553 products for more than 25 years. DDC's design and manufacturing facility is located in Bohemia, N.Y.

SECTION 4:

DISTRIBUTED AND RECONFIGURABLE ARCHITECTURE FOR FLIGHT CONTROL SYSTEMS

DISTRIBUTED AND RECONFIGURABLE ARCHITECTURE FOR FLIGHT CONTROL SYSTEM

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Abstract

New airplanes must meet rigorous requirements of aviation safety, operational reliability, high performance and energy efficiency at a low cost. To meet this challenge, we should optimize current system and take advantage of available technology for the next decade.

This work is aiming at proposing some evolutions for Flight Control System (FCS) and to build alternative FCS low-cost and safe architectures for the next decade with less hardware and software resources.

The main contribution of this paper is twofold. First, we will provide an incremental methodology to give guidelines for architecture optimization. Second, we will present a full distributed reconfigurable architecture for FCS based on smart actuators and digital communication network where all system functions are distributed to simplex Flight Control Computer (FCC) nodes and remote actuator electronics nodes (FCRM). Communication between FCC and FCRM will be based on Airbus embedded communication network (ADCN, Advanced Data Communication Network) [1] and a 1553 bus. We will use ALTARICA language to perform dependability evaluation at architectural level in order to check the effects and benefits of the new architecture on the dependability of FCS.

Introduction

Airplane performance and business pressures related to cost have been the main drivers to change flight control system from mechanical to digital Fly-By-Wire (FBW) design [2]. Technical improvements considered for the future, such as smart actuators/sensors with remote electronics and digital communication, will change drastically avionics architectures design for future commercial and military programs [3,4]. A FBW control system has several advantages over a mechanical system but equipments and architectures proposed for FBW critical systems such as FCS must meet stringent safety and availability requirements before they can be certified. For FCS, the probability of losing an aircraft critical function or of an occurrence of a critical failure must be less than 10^{-9} per flight hour.

Traditionally [5], FCS has used a centralized /federated architecture where a specific fault tolerant computer has performed all processing and authority. This architecture is inherently robust, because it is based on a high level of software and hardware redundancy. However, it can be very costly in terms of space, weight and power, and also wiring requirements between the elements of the system especially for large airplane. This also increases all continuous monitoring of "non-intelligent" components like actuators and sensors that the computers are performing at the present.

Given the high level of redundancy practiced, it seems interesting to try to propose alternative architectures with less hardware and software resources and to take advantage of technical improvements.

In this context, there is a great motivation for future programs to change current flight control architectures to more distributed and better optimized architectures as shown in Figure 1.

FCS architectures will be based on digital technologies and intelligent subsystems and offer many improvements on centralized architectures. They can help to reduce redundancy and the complexity of principal computing elements in FCS through the migration of some functions out of the FCC and the integration of smart subsystems.

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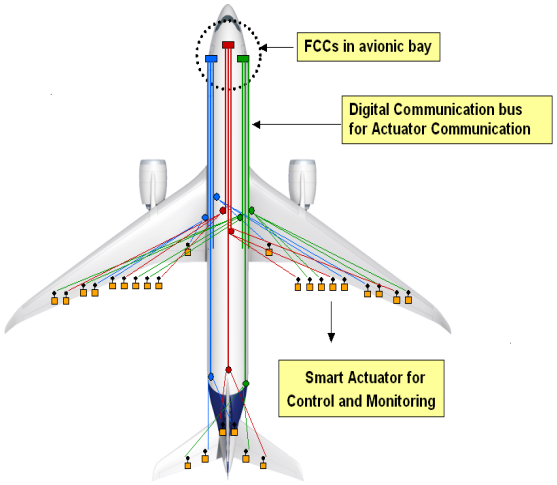

Figure 1. Full Distributed FCS Architecture

In this paper we propose a conceptual fully decentralized and reconfigurable architecture for FCS with architecture optimization and control distribution, where it is possible to use systems resources and new technologies better.

FCS is a very critical system and consequently must be carefully designed and exhaustively checked. We validate the proposed architecture through simulation using ALTARICA language (a high level formal description language) and SDT (System Design Tool) for system safety and reliability assessments.

The paper is organized as follows. This first section has presented flight control systems evolutions. The second section analyzes the state of the art of current FCS architectures. The third section gives an overview of an incremental methodology for architecture optimization. The fourth and fifth sections describe and analyze massive voting architecture, and illustrate the use of ALTARICA for dependability evaluation.

State Of The Art Of Current FCS And Their Requirements

Traditionally, FCSs have used a centralized and federate architecture where a specific computer has performed all processing and authority. In the context of our work we have analyzed a set of FCS architectures. The first subsection presents the Airbus and Boeing design. The second subsection presents a short analysis of redundancy, and the last subsection presents the system requirements identified.

Airbus And Boeing Design

The Airbus flight control system is based on many self-checking flight control computers [6]. Each FCC is composed of two software variants or units (command and monitoring unit) [7] whose results are compared. The command unit and the monitor unit are separated channels within a single computer.

Each channel has separate hardware and different software. If the results of the channels don't correspond (as checked by a comparing function) or are not produced at the same time then an error is assumed and system control switches to another computer. Computers communicate with each other through point-to-point digital communication in order to manage FCS redundancy taking into account different failure cases.

The Boeing PFCS (Primary Flight Control System) [8] comprises three Primary Flight Computers (PFCs), each of identical design and construction and four analog computers ACE (Actuator Control Electronic).

The PFCs compute control-surface position commands and transmit position commands to ACE via ARINC buses. The ACEs position the control surfaces using actuator systems. The ACE units act as an intermediate stage between the PFC and the pilot and actuators. Each PFC is identified as a channel and is composed of three dissimilar computing lanes [9]. Primary flight control system lines have all the same input signals and are all active. Their outputs are connected to a voter that compares these signals. Majority voting then chooses the correct signals. 2-out-of-3 voting can mask the faulty module. Each actuator is controlled by a single ACE and each ACE can receive orders from all PFCs.

All Flight Computers in Airbus and Boeing design are installed in the avionics bay and are connected directly by individual wires to all relevant sensors/actuators through point-to-point links. The relations between flight computer and actuators are arranged so that different computers control each actuator with priority order, so loss of a single computer will not mean loss of control of that surface.

System Analysis

The analysis of current flight control architectures shows that the design and implementation of such a safe system are realized through the combined use of redundancy and diversity (software redundancy) to minimize the probability of common mode failure between redundant units. It also shows that level of redundancy is very important.

This "over-redundancy" is justified by the need for a demonstration of safety and operational reliability especially for commercial airplane, which is guided by regulation authority and economic pressure.

However, given the high level of redundancy practiced, it seems interesting to try to propose alternative architectures on less hardware and software resources. To conduct this exercise, we first have to identify and classify all requirements to be met by flight control system architecture.

System Requirements

Safety And Civil Aviation Regulations

Fail-safe design concepts [10] are required by civil aviation regulations. The system has to meet the FAR/JAR 25 (Joint Aviation Authority/Federal Aviation Regulations) requirements for certification [11, 12]. It means that for a planned or existing system it must imperatively be possible to demonstrate its level of safety in order to be accepted by the authorities. This is to show that the system is robust against any considerable failure or combination of failures [13, 14].

The flight control system usually has two types of dependability requirements:

- Integrity: the system must not output erroneous signals. In particular, Flight Computer should not send incorrect information to the actuators.
- Availability: the system must have a high level of availability.

Economic Requirements

Operational reliability is very important for airlines to stay competitive. FCS must have sufficient redundancy of software and hardware components so that a failure will not disrupt the availability of the system services. The availability objective of flight control systems is to be able to dispatch the aircraft with one or more components failure, so aircraft may take off with one defective equipment. The airplane will have a large operational availability and relatively few maintenance hours, to enable airlines to organize easy maintenance for their fleet. It is required that the FCS be still usable with the expected level of safety, even if an equipment failure could not be repaired for several days (ie. before returning for maintenance). The number of successive flights under such conditions is limited.

Radiation Environment

Electromagnetic radiation should also be considered. The radiation must not affect data communication associated with the Fly-By-Wire system. Particularly, the system must be especially protected against over voltages and under voltages, electromagnetic aggressions, and indirect effects of lightning.

Manufacturing Faults

The choice of technological components and process development strategies [15] (quality control, rules for equipment design) are important factors to control reliability. Despite the precautions taken, a decline in production quality may occur in several defective components (less reliable). Thanks to the inclusion of additional redundancy, FCS provides sufficient margins to tolerate this kind of fault [16].

Incremental Methodology

Analysis of existing FCS architectures, and their requirements, lead us to introduce a brief overview of an incremental methodology to build a new architecture based on progressive requirements injection and distribution of the function of the system [17]. The question we are trying to solve is: what level of redundancy has to be achieved?

Flight control systems are complex. There are several subsystems (flight control computer nodes, actuator nodes, communication network,) with functional and structural dependency. Each subsystem has different timing and dependability requirements with different levels of criticality. For these reasons, a structured approach is necessary for architecture optimization. It is more natural to proceed in a gradual manner by building and validating the architecture step by step, this is the objective of the incremental methodology: starting

with a basic block architecture and then taking into account each requirement, which results in duplication of hardware or/and software or function migration. This approach allows us to analyze the real needs and justify each additional hardware and software cost.

The steps in the incremental methodology process are:

- Step 1: identification of all subsystem boundaries and requirements. At the start, we advise to define all principal subsystems without looking for their dependency.
- Step 2: allocation of tasks (system functions) under an optimizing criterion of the central control because FCCs are complex, big and expensive.
- Step 3: definition of safety objective per subsystem. Safety objective is the probability of system failure due to a subsystem failure.
- Step 4: choice of basic block architecture to meet functionality. Firstly, only necessary functional capabilities must be realized. A single component should be sufficient (one computer, one actuator or one switch…).
- Step 5: classification of requirements based on their criticality.
- Step 6: injection of the first requirement.
- Step 7: assessment of quantitative reliability and preliminary evaluation of the objective of the probability (we can use assumptions for calculation formula).
- Step8: use of hardware/software replication, function migration or reconfiguration to meet the probability objective with the first requirement.
- Step 9: iteration over all requirements.
- Step 10: iteration over all sub-functions.

This approach is part of a complete safety process methodology that allows us to define a new safe architecture for a complex real time safety-critical system.

Example

In this subsection we apply our approach on the most critical subsystem of the FCS: the flight control computer system where a single simplex FCC can handle all system processing and monitoring. But FCS must be designed to continuously provide service despite failure, so we need redundancy.

Flight control computer primary architecture is given by the necessary basic simplex node and software required for system functionality (laws computation). Extra hardware is then added to the architecture as hardware and software replication or dynamic software reconfiguration in order to meet the safety and availability requirements due to permanent and transient faults. In our approach, it is possible to reconfigure one or more FCC to meet dissimilarity requirement.

Dynamic software reconfiguration is a useful mechanism to adapt and maintain systems dissimilarity without need of other forms of reliability, such as redundancy. We consider that the probability objective is 10^{-9} per flight hour for the flight control computer system and the failure rate of one computer does not exceed 10^{-4} per flight hour. As a result, we are in need of additional redundant components, so other requirements should be injected.

We use assumptions to simplify the calculations of probability formula. The formula for probability calculation changes with the number of redundant equipments used to build a fault tolerant architecture and the MMEL (Master Minimum Equipment List) condition: for 3 BFCC primary architecture, and taking into account three requirements (integrity, availability and operational reliability). The probability is calculated as follows:

$$P1 \cong 3\lambda 1T0 \times 2\lambda 1T0 \times \lambda 1$$

Abbreviations And Acronyms

- BFCC: Basic Flight Control Computer
- MTBF: Mean Time Before Failure
- P: Mean Probability per flight hour for the system total failure.
- T1: Maintenance interval or MMEL rectification interval: number of flight hours performed without maintenance action.

- T0: Mean flight time
- λ1: Failure rate of FCC (λ1 = $MTBF^{-1}$).

The probability of system failure is simply the sum of individual BFCC failures probabilities. The formula is organized in three parts:

Initially, 3 active components exist. It is accepted to lose one component before or during the flight. This can occur during the time limit T1. The aircraft may take off with defective equipment. The number of successive flights under such conditions is limited to ten (T1 = 100 hours: 10 flights of 10 hours).

The aircraft performs 10 successive take-offs with BFCC 1. During the flight, it is tolerable to lose another computer; this can exist during time T0.

BFCC 1 failure must occur at first, followed by BFCC 2, and finally BFCC 3 failure. Last failure must occur during the flight to lose the whole system.

The last failure is catastrophic and should be shown to occur at a rate less than or equal to $1x10^{-9}$ per flight hour (combined with former failures) for computer flight control systems architecture. System failure must occur after triple combination failure (loss of three BFCC) without repercussion phase. P1 must be less than 10^{-9} per flight hour.

Under MMEL (Master Minimum Equipment List), P2 must be less than 10^{-8} per flight hour and P3 must be less than 10^{-9} per flight hour.

$$P2 \cong 2\lambda 1T0 \times \lambda 1$$

$$P3 \cong 3\lambda 1T1 \times 2\lambda 1T0 \times \lambda 1$$

This example shows that incremental methodology allows us to reduce the number of FCC nodes in the architecture.

Future Architecture For FCS

Currently, smart element (actuator and sensor) on current flight control system is capable of pre-processing data in digital form. Smart actuator comes with their own computational elements and will be equipped by flight control remote modules (FCRM). FCRM is typically an Application-Specific Integrated Circuit (ASIC) or a Field Programmable Gate Array (FPGA). But for commercial flight control system, overall critical function and authority is still retained within the primary flight computer. In other words, the FCC still makes all the important (safety critical) decisions and the smart subsystems interact intelligently with it.

Distributed architecture offers a number of improvements over centralized architectures by re-hosting data processing and control functionality from the primary computational elements into other subsystems and making them more and more intelligent. Next subsection presents a distributed architecture, with migration of some functions from FCC to FCRM nodes. Distribution refers to distribution of computing power, control and monitoring.

General Description Of The Massive Voting Architecture

With distributed flight control architecture, there are several possibilities to allocate the task of control laws and logic (monitoring, fault detection and handling). Our optimization strategy to build the massive voting architecture implies that redundancy management or voting and logic should be allocated to actuators nodes or shared between computer and actuator nodes. This give a high degree of hardware fault detection for both actuator and computer fault without extra hardware. Most voting algorithms do not demand high processing capability, so processing in the actuators nodes is not considered a limiting factor of a future distributed architecture on flight control systems. The massive voting architecture benefits from digital communication and new technology for smart actuators:

- Digital communication provides broadcast communication between FCC and actuator nodes.
- Digital communication is rapid responding to remote terminal especially for large airplane.
- Electronic for smart actuator can be designed with high degree of embedded computing capability.

We considered an architecture with N simplex, independent computer nodes, grouped into two groups (of N/2 elements). In this architecture, we

replicate the main hardware unit N times and their outputs are constantly voted by a massive voting algorithm implemented in M distributed actuator nodes. In some cases, there are two actuators per surface and one FCRM per actuator. Communication between FCC and FCRM will be based on Airbus current embedded communication network (ADCN, Advanced Data Communication Network) and a 1553 bus.

FCC are simplex, but FCRM are duplex (command/monitor architecture). Each FCRM has it own voter. FCCs have two software variant (S1 and S2) and two hardware variant (H1 and H2). Each voter on each FCRM needs to collect the output orders of all FCC nodes and of the two plane sides as shown in Figure 2.

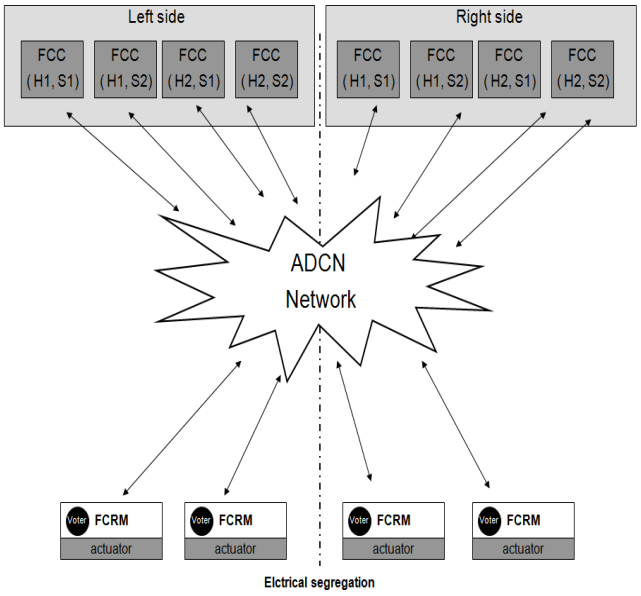

Figure 2. The Massive Voting Architecture

FCCs are connected to the ADCN network and can communicate to all actuator nodes trough a multi-master broadcast configuration. All FCC intra-communications are removed. Communication between flight control computer nodes and actuators nodes is organized as follows.

- Firstly, all FCC nodes calculate flight control laws and control-surface position commands for all actuators nodes (spoiler, elevator…) and then broadcast their message on the bus.
- Each actuator receives N/2 messages from each computer group at every application cycle (control law computation frequency).
- Secondly, each FCRM node achieves a massive voting to select a good order. In absence of fault all correct working voter should agree.

The voter may use different algorithms in the voting process of selecting correct order [18, 19].

Fault Handling

In massive voting architecture most fault handling is taken care of in actuator nodes. With several actuator nodes, each of them providing a feedback, a high degree of fault detection and fault location can be achieved.

Because FCC nodes are simplex, this requires a fault detection function to detect the faulty situations. First simple fault detection mechanism in FCC nodes use the output signal for inner consistency checking like parity checking or watchdog timers. The second fault detection mechanism is based on FCRMs feedbacks. If a fault occurs in an actuator node, that node will either be fail-silent or broadcast faulty command-words since the actuator has a command monitoring architecture. The command channel ensures the function allocated to the FCRM (voting, monitoring). The monitoring channel ensure that the command channel operate correctly.

Simulation

Up to 80 percent of the total cost of the life cycle of an airplane is set during the early design phase, so mistakes on architectural decision are expensive. To minimize risks, dependability analysis should be introduced early in the design process, and decision should be based more and more on simulation.

This section discusses modeling and dependability assessment of massive voting architecture with ALTARICA language. All dependability measures can be evaluated based on ALTARICA model but in this paper and for FCS we are just interested in safety and availability. We need to verify the effect of the massive voting architecture on system requirements, and application.

ALTARICA Language

ALTARICA is a formal language developed at LaBRI (Laboratoire Bordelais de Recherche en Informatique) jointly with French industrial partners (especially Dassault Aviation and Airbus) in order to model safety critical systems. ALTARICA is used for modeling both functional and dysfunctional behaviors of systems. ALTARICA is widely used by aeronautical industrialists [20].

Thanks to the language well defined semantics and syntax, safety assessments of ALTARICA models can be analyzed by numerous reliability or validation tools. Moreover, its capacity to realize compositional and hierarchical models is a great advantage when complex systems must be modeled [21]. An ALTARICA model is composed of several components linked together. Each system component is modeled by a node. A node is defined by three parts:

- declaration of variables and events
- definition of transitions
- definition of assertions

Most of the events of an ALTARICA model, that describe failure propagation in a system, represent failure modes of the components of the system. These events are mainly stochastic events: probability laws can be associated to them and later be used to evaluate the enforced quantitative requirement. The means of analysis on ALTARICA model are:

Interactive simulation:

- possible events may be triggered
- component icons and links color are updated

Automatic generation for a selected output value of:

- Fault tree
- Minimal Cut Sets (MCS)
- Minimal Sequence Sets (MSS)

Model-Checking:

- given a requirement, exhaustive exploration of reachable states in order to find a state where the requirement is not fulfilled
- production of a counter-example if the requirement is not fulfilled.

Application On Your Architecture

Architecture Modeling

Using SDT (System Design Tool) workshop of Airbus, we designed and implemented, a small ALTARICA model of the massive voting architecture for experimentation. In our simulation scenarios N is equal to six. The simulation model includes all systems communication, computing nodes (FCC and FCRM), electrical system and control surfaces and their failure modes to study failure propagation in the model as shown in Figure 3.

Massive voting architecture component has several failure modes:

- total loss
- detected erroneous functioning
- undetected erroneous functioning
- erroneous acquisition of data
- erroneous transmission on network

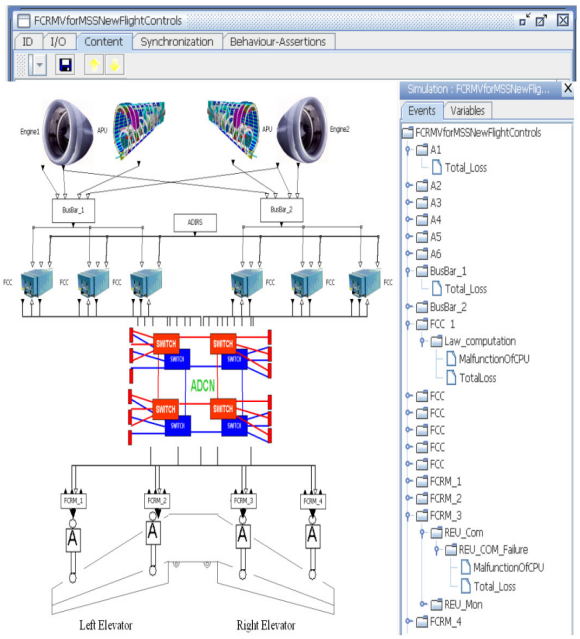

Figure 3. An Architectural Altarica Model

ALTARICA component model is composed of:

- A textual description (flow and events impacting the current state of the component) to describe both functional and dysfunctional behaviors as shown in Figure 4.

```
node S
  state
    status : {correct, lost};
  flow
    PowerFromElecGen: bool , in;
    ActivationOrderReceived: bool , in;
    OrderToSc: {correct, lost} , out;
  event
    sleeping_loss, acting_loss;
  trans
    PowerReceived and status = correct
            and not Activation |- sleeping_loss -> status := lost
    PowerReceived and status = correct
            and Activation |- acting_loss -> status := lost;
  assert
    OrderToSc = case {PowerReceived : status;
                      else lost};
  init
    status := correct;
edon
```

Figure 4. Altarica Node Textual Description

- A graphical representation (flow and icons updated to reflect the current state) as shown in Figure 5 of FCRM model.

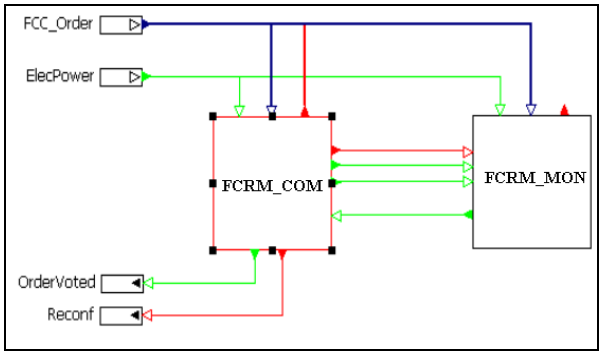

Figure 5. FCRM Node Graphical Representation

Safety Assessment With ALTARICA

After having modeled the architecture, we can perform dependability evaluation in order to check the effects and benefits of the new architecture on the dependability of FCS. We check the effect of failure occurrences on the system architecture by using SDT graphical interactive and automatic simulator.

Firstly, we use interactive simulation to validate each component behavior separately in order to verify system behavior and reaction in case of failure occurrence (by injection fault). Interactive simulation allows us to look at the consequence of each failure event in the architecture model (icons or textual updated to reflect the current state).

In test case one, the FCC1 sent a fault command to actuator nodes: undetected erroneous functioning event is trigged. Simulation shows that FCC1 failure has no influence in the surface control since the vote masks the faulty value and delivers the correct one with an negative acknowledgment to faulty FCC as shown in Figure 6.

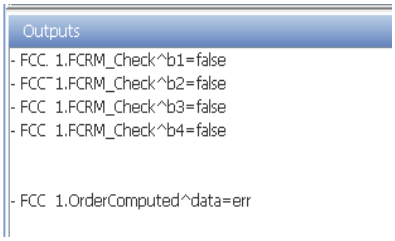

Figure 6. FCC Textual Simulation Result

Secondly we use automatic simulation to search MSS (minimum size sequence) or MCS (minimum cut sets) for event leading to FC for exhaustive validation.

The process for automatic simulation is as follows. First, the analyst defines all unsafe situations (called Failure Condition: FC) and associate a classification (minor, major, hazardous or catastrophic) and safety requirements (qualitative and quantitative). Then, he models the FC with a specific component (called observatory) integrated to the architecture model. Finally, SDT tool searches automatically all minimal combinations of failures leading to a given FC and compute the probability of FC. Architecture is valid only if all FC requirements are met. The result of automatic simulation for the "FC = Loss of both elevator control" must be less than 10^{-9} per flight hour, and it is shown in Figure 7.

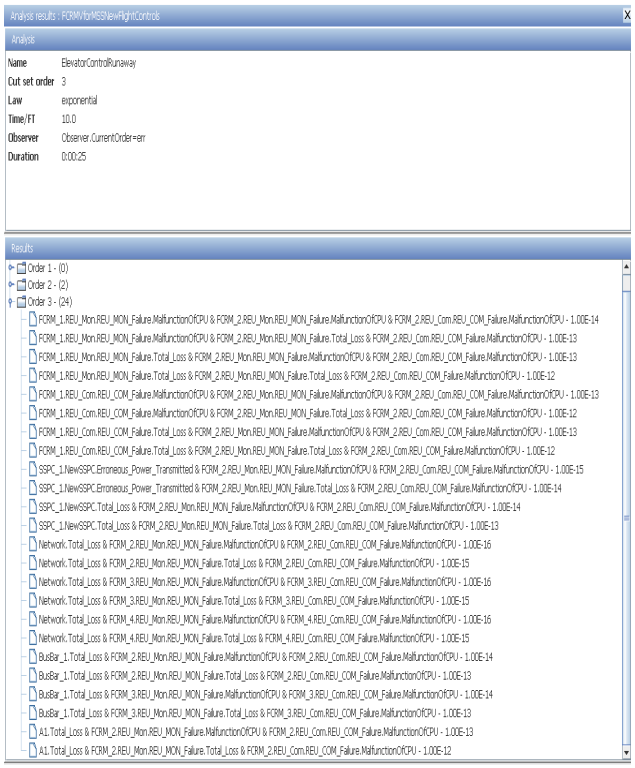

Figure 7. Loss of Both Elevator Control

Conclusions

Distributed FBW systems are the last step in the evolution of the traditional airplane FCS architectures. The evolution of microelectronic and communication technologies will continue to have an extreme influence on the FCS architecture.

This paper has shown the way that one could use so that using digital communication and smart actuators can eliminate the centralized architecture and reduce the number of centralized computers to achieve low cost that is vital for new aircraft without dependability degradation. Digitally distributed FBW architectures offer many improvements over centralized architecture. They can help to reduce redundancy and the complexity of principal computing elements in FCS architecture through the migration of computation functionality out of the FCC and the integration of smart subsystems. The processing tasks realized by central flight computers are also simplified, so that critical safety computing can now be more easily accomplished by low cost standard computing resources like IMA [22] or COTS (Commercial Off-The-Self) [23].

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28th Digital Avionics Systems Conference
October 25-29, 2009

SECTION 5:

HIGH PERFORMANCE 1553

High Performance 1553

Abstract

The U.S. Air Force is currently in the process of developing a revision to MIL-STD-1553 that will provide additional digital communication bandwidth beyond MIL-STD-1553B's 1 Megabit per second (Mbps) rate. The proposed revision to MIL-STD-1553 (referred to as MIL-STD-1553C) is targeting 200 Mbps as a baseline data rate. This paper explores the feasibility of the U.S. Air Force's proposed revision to MIL-STD-1553 based on studies conducted by Data Device Corporation (DDC). A combination of empirical and theoretical methods is used to determine if a MIL-STD-1553B network contains sufficient capacity to support the proposed 200 Mbps data rate. The results of DDC's analysis is that for some MIL-STD-1553 buses there is sufficient bandwidth to implement a broadband system in which legacy 1 M bps 1553B waveforms could coexist with new 200 M bps waveforms, thus providing an incremental high speed communication channel to existing MIL-STD-1553 buses.

Keywords: MIL-STD-1553, avionics, military, data bus, high speed, broadband, capacity

Introduction

MIL-STD-1553 is a robust serial data bus that has served as the primary command and control data network on board military aircraft for the last three decades. MIL-STD-1553's characteristics of high reliability, high availability, fault tolerance, and highly interoperable have made it the data bus of choice for avionics systems. MIL-STD-1553 is still well suited for a large number of avionics applications; however, there are emerging requirements for high speed communication beyond MIL-STD-1553's 1 Mbps rate.

Traditional avionics system have been implemented based on what is referred to as a federated architecture which consists of a series of independent subsystems which are interconnected with a fairly low speed command and control network (i.e. MIL-STD-1553). Information is processed with each subsystem and the results of the processed data are shared with other subsystems on an as needed basis. In general the amount of data passed between subsystems had been relatively low.

The advent of network enabled warfare and the increased desire to fuse sensor data from multiple sources (including off board data from other platforms or UAVs) is increasing the demand for high speed communication between subsystems on aircraft. Satisfying this demand for higher bandwidth communication on existing aircraft requires that either new cabling is installed or higher data rates are run over existing cabling. The implementation of new high speed interfaces becomes an economic tradeoff between the costs of adding additional cabling and associated electronics versus the cost of updating the existing electronics to increase the data rates on the existing MIL-STD-1553 buses. The US Air Force has estimated that it would cost approximately one million dollars to rewire a fighter aircraft to supplement or replace the MIL-STD-1553 cabling[1].

The U.S. Air Force is currently engaged in the development of a revision to MIL-STD-1553 (from Rev B to Rev C) for the purpose of adding a new high bandwidth waveform that will provide 200 Mbps (or higher) bandwidth on existing 1553 buses,

such that it will not interfere with legacy 1553 communication. This paper presents the results of testing conducted by DDC that support the feasibility of the U.S. Air Force's goal of expanding the bandwidth of MIL-STD-1553.

MIL-STD-1553 Infrastructure

MIL-STD-1553 Network

MIL-STD-1553 specifies a multi-drop linear time division multiplexed data bus (refer to Figure 1)[2]. The topology of a MIL-STD-1553 bus consists of a main transmission line that is terminated at both ends with a resistive load equal to the characteristic impedance (defined to be in the range of 70 to 85 ohms). Each terminal contains a transformer for the purpose of providing galvanic isolation. A terminal may be connected to the main bus using either a direct or transformer coupled connection. Direct coupled connections require that the terminal include a pair of fault isolation resistors in series with the isolation transformer. Transformer coupled connections utilize a bus coupler which contains an impedance matching transformer in addition to a pair of isolation resistors. The vast majority of 1553 implementations utilize transformer coupling. MIL-STD-1553B Notice 2 states "for Army and Air Force systems, only transformer coupled stub connections shall be used"[3].

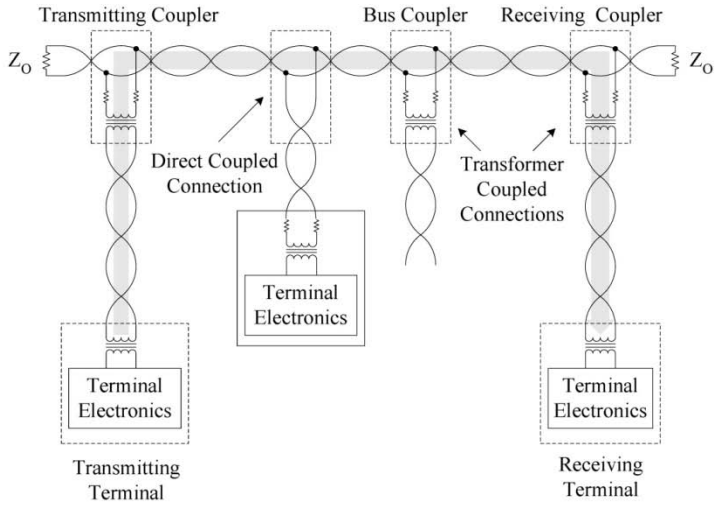

Figure 1. Transmit data path from a transmitting to a receiving 1553 terminal

The signal path of interest is from a transmitting terminal to a receiving terminal. A transmitted waveform first travels down the stub cable to the first bus coupler, then passes through the bus coupler to the main bus. The signal then travels down the bus passing through several bus couplers until it reaches the receiving coupler The signal finally passes through the receive coupler and up the stub cable to the receiving terminal (refer to Figure 1). It has been shown in previous papers that the loss through the coupling transformers can be extremely high for signals beyond the MIL-STD-1553 passband[4].

MIL-STD-1553 Waveform Characteristics

MIL-STD-1553 utilizes Manchester II biphase encoding which, theoretically, can be implemented as a phase modulated 1 MHz signal. The theoretical bandwidth requirement for a 1 Mbps 1553 waveform is 2 MHz. A practical implementation of a MIL-STD-1553 transmitter will consist of higher frequency harmonics of the fundamental 1 M Hz signal. The higher frequency harmonics of a MIL-STD-1553 waveform will dictate the time domain shape of the pulses.

Figure 2 illustrates the time and frequency domain content of a 1 Mbps Manchester encoded waveform for various cutoff frequencies. The first pair of plots in Figure 2 show the time domain waveform for a Manchester waveform that is band limited to 2 MHz, and thus contains only the fundamental modulation frequency. The remaining pairs of plots in Figure 2 show the time domain waveform of the Manchester waveform with higher cutoff frequencies (i.e. more harmonic content).

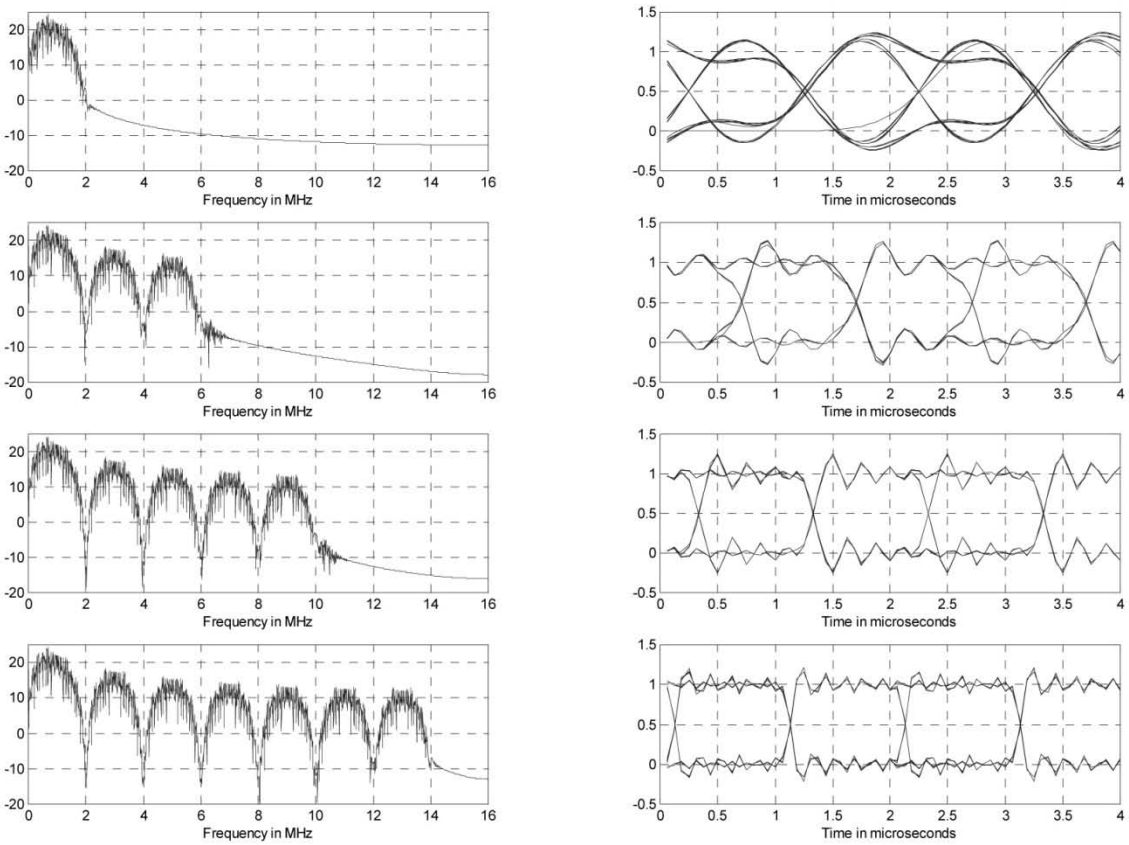

Figure 2. Frequency and time domain of Manchester encoded waveforms

As the cutoff frequency of the 1553 transmitter is increased, the time domain plot changes from a sinusoidal waveform to a trapezoidal waveform. MIL-STD-1553 does not specifically define the harmonic content requirement of a transmitted waveform other than to define the rise and fall time to be in the range of 100 to 300 nanoseconds. It can be seen from Figure 2 that there is a relationship between harmonic content in the frequency domain with rise and fall time in the time domain. MIL-STD-1553's minimum rise time (100 ns) will produce a waveform similar to the last plot in Figure

2, which contains significant harmonic content above the passband of the modulated signal. The range of rise and fall time was most likely selected to facilitate simpler transmitter designs while still meeting the intended performance requirements given the transmission line characteristics of the bus. The implication for a broadband system is that legacy MIL-STD-1553 waveforms may contain significant high frequency content.

Measurements

The key parameter required to calculate the capacity of a network is the signal to noise ratio (SNR). An analytical prediction of SNR requires a model that quantifies signal and noise levels independently. Figure 3 illustrates a basic communication model for additive noise that shows the relationship between the transmitted signal (S_T), the received signal (S_R), and noise (N)[5]. The model assumes that a received signal consists of a transmitted signal that is distorted based on the response of the channel through which it travels. Noise is then added to the received signal and presented to the receiver.

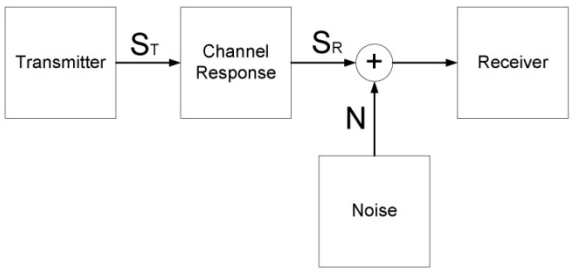

Figure 3. General communication additive noise model

DDC conducted a series of measurements on MIL-STD-1553 networks to characterize each of the elements in the SNR model. EMI tests were conducted to determine the maximum transmit signal level that could be produced by a transmitter and remain compliant to the radiated emissions levels in MIL-STD-461. Insertion loss measurements were conducted to characterize the distortion introduced by a typical 1553 network. Finally noise measurements were conducted to characterize the various noise sources which are present in a 1553 system.

Transmit Signal Level

A MIL-STD-1553 network was built for test and measurements purposes (refer to Figure 4). This networked was tested to RE-102, radiated emission electric field 10 kHz to 18 G Hz, defined in MIL-STD-461. The test network is believed to be representative of a worst case 1553 network consisting of a 300 foot bus with 32 stubs. The couplers were mounted on a copper ground plane (refer to Figure 5).

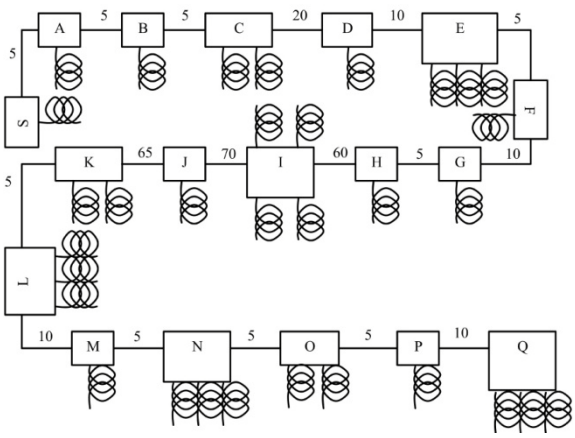

Figure 4. Worst case test network

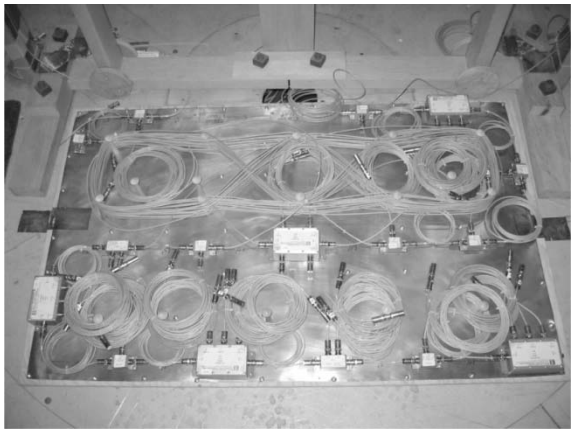

Figure 5. 1553 network on copper ground plate

The 1553 test network was placed in the EMI chamber and covered with grounded foil. Various lengths of cable from different portions of the network (both stub sections and bus sections) were placed on a wooden rack with the specified spacing from the ground plane and the measurement antennae. An arbitrary waveform generator was used to create a number of transmit waveforms with various transmit spectrums. The frequency response of one of the transmit waveforms is shown in Figure 6. The electric field emissions for one of the tests conducted is shown in Figure 7.

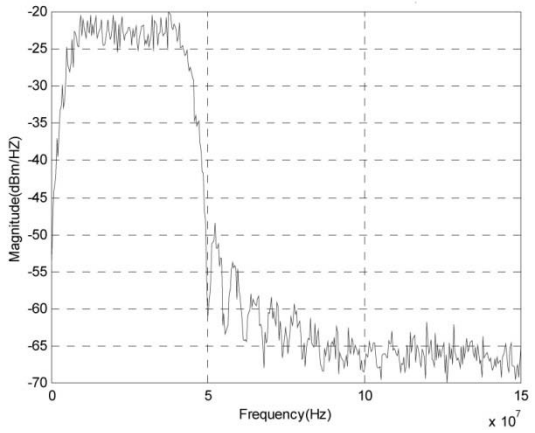

Figure 6. Spectrum of one of the EMI test signals

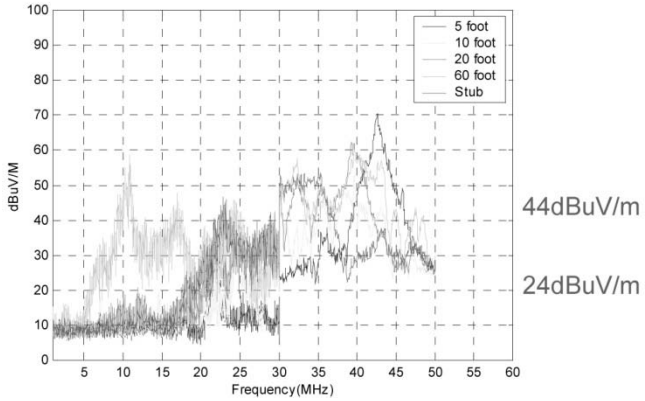

Figure 7. Emissions on various lengths of cable

The results of the emissions tests were used to formulate a transfer function (as a function of frequency) for predicting the radiated electric field strength as a function of the power density of the transmitted waveform on the bus. It is assumed that the emission level will scale linearly with the transmitted waveform power level. This transfer function was then used to calculate the maximum the maximum transmit signal level based on a radiated field strength that is less than the limits defined in MIL-STD-461. This calculated signal level represents the transmitted signal level (S_T) in Figure 3.

Received Signal Level

A network analyzer was used to measure the insertion loss of several channels within various MIL-STD-1553 buses. The network analyzer applies a test signal to one end of the channel and measures the response at the other end. The network analyzer sweeps the test signal over a frequency range to generate the response curves. Figure 8 illustrates the magnitude of the channel response as a function of frequency for DDC's "half test bus" and a "real bus" on a production aircraft. The half test bus consists of half (i.e. 16 terminals instead of 32 terminals) of the network defined in Figure 4. This half test bus is believed to be representative of a typical 1553 bus.

The results of the insertion loss measurements were used to formulate a t ransfer function for the channels. These transfer functions were then applied to the transmitted signal (S_T) calculated in section 3.1 to calculate the received signal level (S_R) for each channel.

Figure 8. Insertion loss for various channels

Noise Level

A MIL-STD-1553 network contains numerous sources of noise including thermal noise, EMI susceptibility from wideband and narrow band sources, and impulse noise. In addition to these classic noise sources, the legacy MIL-STD- 1553 waveforms will be presented to the broadband system as an additional noise source. The results of various noise measurements have shown that the power level of the MIL-STD-1553 harmonics is higher than the other sources of noise and as such MIL-STD-1553 will be treated as the dominant noise source for the purpose of the capacity estimates.

Spectrum analyzer measurements were made on one of DDC's MIL-STD-1553 transmitters to quantify the relative signal power of the high frequency harmonics in a legacy MIL-STD-1553 waveform. Figure 9 and Figure 10 illustrate the spectral content of the 1553 waveform with a constant data pattern.

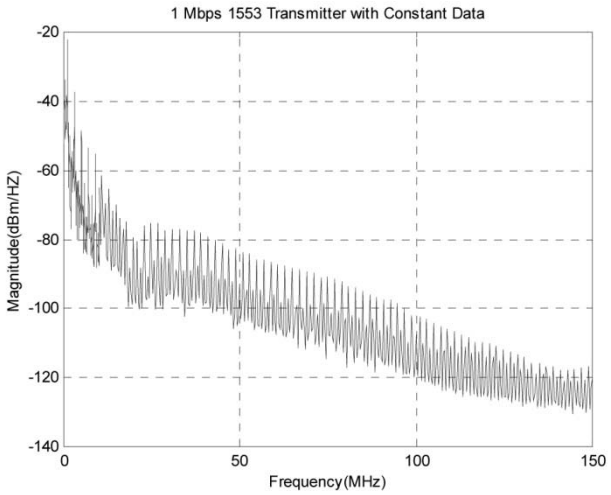

Figure 9. Spectrum of 1 Mbps 1553 waveform with constant data (0 to 150 MHz scale)

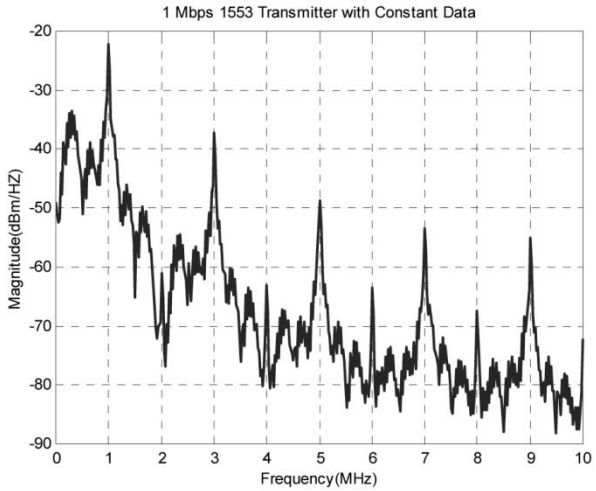

Figure 10. Spectrum of 1 Mbps 1553 waveform with constant data (0 to 10 MHz scale)

Figure 11 and Figure 12 illustrate the spectral content of a 1553 waveform with random data. Comparing the two 1553 transmit waveforms reveals that the spectrum of the 1553 waveform with constant data contains very narrow spikes with a relatively high peak while the spectrum of the waveform with random data produces a more normal distribution within each harmonic and results in a lower peak spectral power. Comparing Figure 10 and Figure 12 shows that the peak at 9 MHz is approximately 10 dB higher for a constant data pattern than the peak for a random data pattern. MILSTD-1553 does not make use of a scrambler and as such there will be a mixture of constant data and some random data based on the nature of the data content.

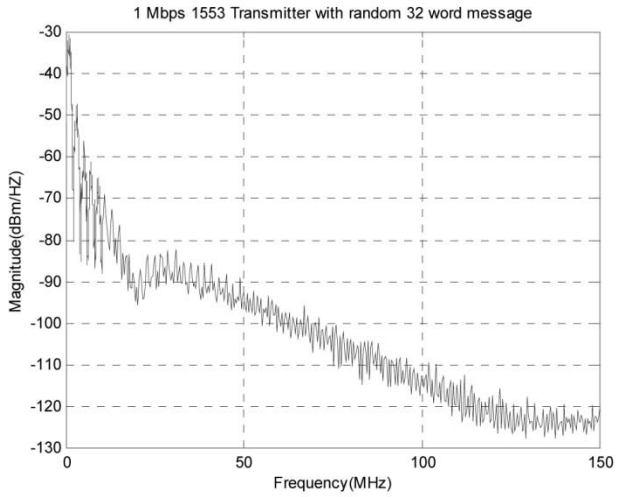

Figure 11. Spectrum of 1 Mbps 1553 waveform with random data (0 to 150 MHz scale)

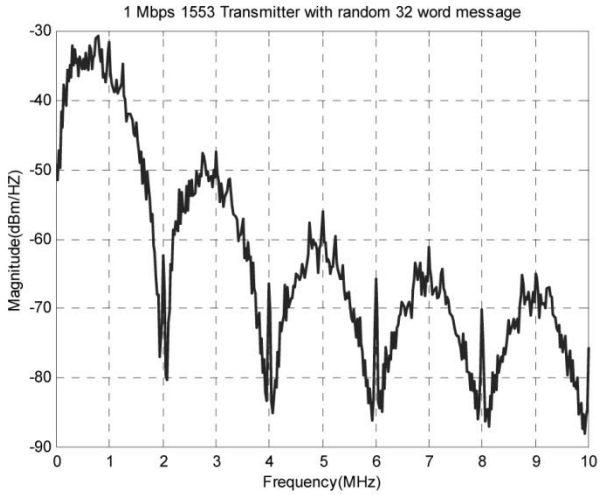

Figure 12. Spectrum of 1 Mbps 1553 waveform with random data (0 to 10 MHz scale)

Figure 13 summarizes the spectrum on various buses with legacy MIL-STD-1553 operating. These measurements reveal that MIL-STD-1553 waveforms contain significant harmonic content up to 10 MHz and even has some content up to 30 MHz. The noise spectral densities shown in Figure 13 represent the noise component (N) in Figure 3 and can be used in calculating the SNR of the system.

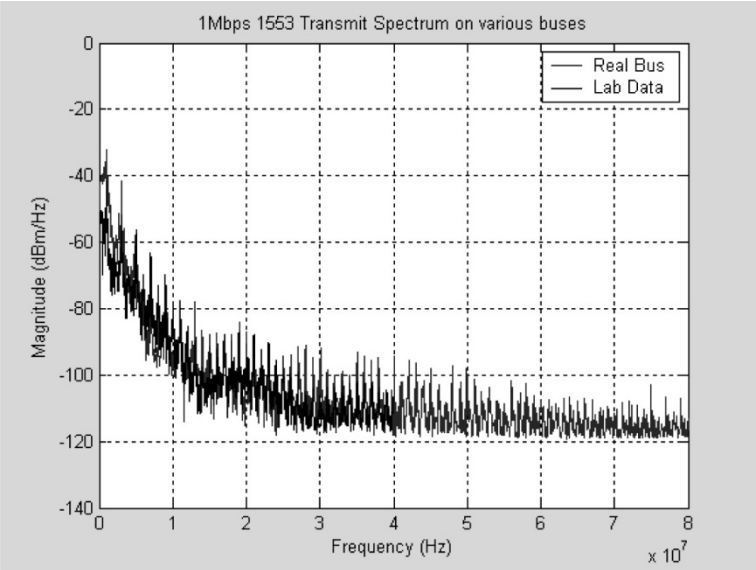

Figure 13. Various 1553 transmit spectrum measurements

Analysis

The signal and noise levels of a broadband system were derived in the previous section. These values can now be used to calculate the overall signal to noise ratio of the system. The SNR needs to be calculated over a defined frequency band. For the purpose of this capacity estimate 30 MHz was chosen because the resulting signal to noise ratio was reasonable and a design using this bandwidth could be realized using existing state of the art technology. Shannon's equation was used to predict the capacity of the measured channels (see Equation 1). This equation includes a factor, K, which represents the performance gap between an uncoded system and the Shannon limit. Selection of the value of K is based on experience with the achievable performance levels of various modulation techniques versus the theoretical Shannon limit.

Equation 1. Capacity Prediction

$$C = \int_{f_1}^{f_2} \log_2 \left(1 + \frac{S_X(f)\left|H(f)\right|^2}{N_0(f) \cdot K} \right) df$$

Capacity predictions were made based on the two sets of measurements. The first capacity estimate is based on the "Half test network" (a lab network consisting of 16 stubs as illustrated in Figure 4). The second capacity estimate is based on measurements made on a bus in real aircraft. The results of the capacity estimates are summarized in Table 1.

Table 1. Capacity estimates for various network configurations		
Bus Configuration	**Bandwidth**	**Shannon Capacity**
Half test network	30 MHz	202 Mbps
Real bus	30 MHz	232 Mbps

Conclusion

The measurements and analyses presented in this paper show, for the buses that were measured, that there is sufficient bandwidth within the channels to support in excess of 200 Mbps. The testing revealed that the channels are very lossy and that legacy MIL-STD-1553 waveforms produce a significantly high noise level in the frequency range above the 1553 passband. An implementation of a high bandwidth system will need to be able to compensate for distortion in the channel and will have to operate with a high noise level. It is believed that this type of high bandwidth system could achieve data rates over legacy MIL-STD-1553 buses in excess of 200 M bps while operating concurrently with legacy MIL-STD-1553 waveforms.

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Data Device Corporation is recognized as an international leading supplier of high-reliability data interface products for military and commercial aerospace applications since 1964 and MIL-STD-1553 products for more than 25 years. DDC's design and manufacturing facility is located in Bohemia, N.Y.

SECTION 6:

DDC’S A350 PRESS RELEASE

PRESS RELEASE

Airbus Chooses DDC's MIL-STD-1553 Components for A350 XWB Flight Control!

Bohemia, New York (March 2010) Data Device Corporation (DDC) has been selected by Airbus to supply MIL-STD-1553 components for its new generation A350 XWB aircraft. Considered a standard, MIL-STD-1553 has caught the attention of commercial aircraft manufacturers, such as Airbus, who seek to capitalize upon 1553's inherent reliability, robustness, maturity, and superior EMI performance.

Airbus based its selection on DDC's decades of experience supplying MIL-STD-1553 data bus boards, components, and software solutions for military, commercial, and aerospace applications, and competitive pricing. Another important consideration was that DDC's products facilitate achieving RTCA/DO-254 Level A certification, a significant factor in the avionics industry.

"DDC was selected for its ability to provide reliable components for critical primary flight control systems, and for its combination of industry expertise, experience, support, and manufacturing capability".

"DDC is proud to have achieved the high standards required by Airbus to become a valued member of the team implementing MIL-STD-1553 solutions on the A350 XWB. DDC looks forward to working closely with Airbus and we are confident that our decades of MIL-STD-1553 experience will be a strong contributing factor to the success of the project", stated Mike Hegarty, DDC's Principal Marketing Engineer.

To learn more click http://www.ddc-web.com/A350/M . To receive a free white paper outlining the evolution of MIL-STD-1553 click: http://www.ddc-web.com/Pub/85/567.ashx

Contact: Chris Stabile, Marketing Communications Manager
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PRESS RELEASE

Data Device Corporation (DDC) is the world leader in the design and manufacture of high-reliability data bus products, motion control, and solid-state power controllers for aerospace, defense, and industrial automation applications. For more than 45 years, DDC has continuously advanced the state of high-reliability data communications and control technology for MIL-STD-1553, ARINC 429, Synchro/Resolver interface, and Solid-State Power Controllers with innovations that have minimized component size and weight while increasing performance. DDC offers a broad product line consisting of advanced data bus technology for Fibre Channel networks; MIL-STD-1553 and ARINC 429 Data Networking cards, components, and software; Synchro/Resolver interface components; and Solid-State Power Controllers and Motor Drives. DDC headquarters and their design and manufacturing operations are located in Bohemia, NY. For more information, visit www.ddc-web.com .

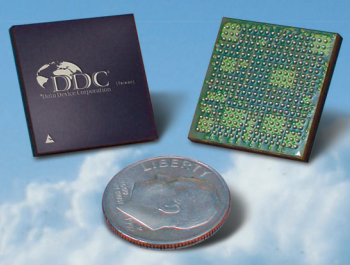
Contact: Chris Stabile, Marketing Communications Manager
E-mail: stabile@ddc-web.com **Tel:** 631 567 5600 ext. 7419

For the First Time...
MIL-STD-1553 goes Commercial

"Airbus Chooses DDC's MIL-STD-1553 Components for A350 XWB Flight Control!"

MIL-STD-1553... The Smart Choice

- Inherently Safe and Reliable
- Less Wiring and Weight
- Superior EMI Performance



Why DDC?

- World leader in MIL-STD-1553
- 62 million hours in flight
- Certifiable to RTCA/DO-254

To read why **Airbus** chose DDC MIL-STD-1553 for the A350 XWB, visit: **www.ddc-web.com/A350/A**

The first choice for more than 45 years — DDC

DDC is the ***world leader*** in the design and manufacture of high reliability data bus products, motion control, and solid-state power controllers for aerospace, defense, and industrial automation.

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Leadership Built on Over 45 Years of Innovation

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Product Families

Data Bus | Synchro/Resolver | Power Controllers | Motor Drives

DDC is a leader in the development, design, and manufacture of highly reliable and innovative military data bus solutions. DDC's Data Networking Solutions include MIL-STD-1553, ARINC 429, and Fibre Channel. Each Interface is supported by a complete line of quality MIL-STD-1553 and ARINC 429 commercial, military, and COTS grade cards and components, as well as software that maintain compatibility between product generations. The Data Bus product line has been field proven for the military, commercial and aerospace markets.

DDC is also a global leader in Synchro/Resolver Solutions. We offer a broad line of Synchro/Resolver instrument-grade cards, including angle position indicators and simulators. Our Synchro/Resolver-to-Digital and Digital-to-Synchro/Resolver microelectronic components are the smallest, most accurate converters, and also serve as the building block for our card-level products. All of our Synchro/Resolver line is supported by software, designed to meet today's COTS/MOTS needs. The Synchro/Resolver line has been field proven for military and industrial applications, including radar, IR, and navigation systems, fire control, flight instrumentation/simulators, motor/motion feedback controls and drivers, and robotic systems.

As the world's largest supplier of Solid-State Power Controllers (SSPCs) and Remote Power Controllers (RPCs), DDC was the first to offer commercial and fully-qualified MIL-PRF-38534 and Class K Space-level screening for these products. DDC's complete line of SSPC and RPC boards and components support real-time digital status reporting and computer control, and are equipped with instant trip, and true I^2T wire protection. The SSPC and RPC product line has been field proven for military markets, and are used in the Bradley fighting vehicles and M1A2 tank.

DDC is the premier manufacturer of hybrid motor drives and controllers for brush, 3-phase brushless, and induction motors operating from 28 Vdc to 270 Vdc requiring up to 18 kilowatts of power. Applications range from aircraft actuators for primary and secondary flight controls, jet or rocket engine thrust vector control, missile flight controls, to pumps, fans, solar arrays and momentum wheel control for space and satellite systems.

Certifications

Data Device Corporation is ISO 9001: 2008 and AS 9100, Rev. B certified.

DDC has also been granted certification by the Defense Supply Center Columbus (DSCC) for manufacturing Class D, G, H, and K hybrid products in accordance with MIL-PRF-38534, as well as ESA and NASA approved.

Industry documents used to support DDC's certifications and Quality system are: AS9001 OEM Certification, MIL-STD-883, ANSI/NCSL Z540-1, IPC-A-610, MIL-STD-202, JESD-22, and J-STD-020.

DATA DEVICE CORPORATION
REGISTERED TO ISO 9001:2008
REGISTERED TO AS9100:2004-01
FILE NO. A5976

The first choice for more than 45 years—DDC
DDC is the world leader in the design and manufacture of high reliability data interface products, motion control, and solid-state power controllers for aerospace, defense, and industrial automation.

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